ApplicationNOTE

GAMRY INSTRUMENTS

Testing Super-Capacitors

Part 1: CV, EIS, and Leakage Current

Introduction

Super-capacitors are energy storage devices similar to secondary batteries. Unlike batteries, which use chemical reactions to store energy, super-capacitors generally store energy through the physical separation of electrical charges.

All super-capacitors consist of two electrodes immersed in a conductive liquid or conductive polymer called the electrolyte. The electrodes are separated by an ionic-conducting separator that prevents shorts.

Compared to a battery, a super-capacitor has the following advantages:

- Higher charge and discharge rates (high power density)
- Longer cycle life (> 100 000 cycles)
- Materials with low toxicity
- Operation over a wide temperature range
- Low cost per cycle

These are offset by some disadvantages:

- Higher self-discharge rate
- Lower energy density
- Lower cell voltage
- Poor voltage-regulation
- High initial cost

Current applications for super-capacitors include:

- Hybrid Electric Vehicles (HEVs)
- Diesel-engine starting systems
- Cordless power tools
- Emergency and safety systems

Many applications use a super-capacitor in parallel with a battery, a combination with a better cycle-life and higher power than the battery alone. For more information read Brian Conway's book on super-capacitor technology.[1]

This application note is the first part of a two-part overview of the electrochemical techniques used to test a super-capacitor device or technology. Part 1 discusses techniques familiar to electrochemists, while Part 2 discusses techniques familiar to battery technologists.

Commercial capacitors were tested to obtain results used in discussion of techniques. The data in this note were recorded on a Gamry Instruments PWR800 system with optional EIS (EIS300) capability. All plots were generated using Gamry's Echem Analyst software.

Items in yellow boxes are specific to Gamry products.

Similar Technology, Confusing Names

A traditional Electrical Double-Layer Capacitor (EDLC) uses electrostatic charge storage to store energy. Electrons in each electrode and ions in the electrolyte form a double-layer capacitor. Typical capacitance of an electrochemical double layer is 20 μF/cm^2. Capacitance of micro-porous carbon with a surface area of 1000 m^2/g can be as high as 200 F/g.

Some devices, which we call pseudo-capacitors, store charge via reversible Faradaic reactions on the surface of one or both electrodes. When electrode voltage is proportional to surface coverage and surface coverage is proportional to state-of-charge, these devices behave identically to capacitors. See Conway's book for details concerning these devices.

Unfortunately, technical papers and commercially available products have used many names for EDLCs and pseudo-capacitors. These include:

- Super-capacitors

[1] B.E. Conway, *Electrochemical Supercapacitors: Scientific Fundamentals and Technological Applications*, New York: Kluwer Academic Press/Plenum Publishers, 1999.

- Ultra-capacitors
- Aerogel capacitors
- Electrical double-layer capacitors

Unless otherwise noted, this note uses the term super-capacitor for all high-capacitance devices, regardless of charge-storage mechanism.

Ideal Capacitors

A capacitor is a storage device for electrical charge. The voltage of an ideal capacitor is proportional to the charge stored in the capacitor:

$$CV = Q$$

C is capacitance in farads;

V is voltage between the device's terminals in volts;

Q is the capacitor's charge in Coulombs, in ampère-seconds.

A capacitor's state-of-charge is easily measured: it is proportion to voltage. In contrast, measuring a battery's state of-charge can be difficult.

The energy stored in a capacitor is:

$$E = \tfrac{1}{2}CV^2$$

E is the energy is joules.

The power drawn from a capacitor during discharge depends on the capacitor's voltage and the electrical current:

$$P = VI$$

P is power in watts;

V is the capacitor voltage in volts;

I is the discharge electrical current in ampères.

An ideal capacitor loses no power or energy during charge or discharge, so the equation above can also be used to describe the charge process. An ideal capacitor with no current flow will store energy and charge forever.

Non-ideal Capacitors

The ideal capacitor does not exist, for real capacitors have limitations and imperfections. The tests in this application note measure these limitations.

Voltage Limitations

The description of ideal capacitors did not mention voltage limitations. Capacitors can only operate within a "voltage window" with both an upper and lower voltage limit. Voltages outside the window can cause electrolyte decomposition damaging the device.

Capacitor electrolytes may be aqueous or non-aqueous. While aqueous electrolytes are generally safer and easier to use, capacitors with non-aqueous electrolytes can have a much wider voltage window.

When this was written, commercial single-cell super-capacitors have an upper voltage limit below 3.5 V. High-voltage devices have multiple cells in series.

All commercial super-capacitors are specified to be unipolar: the voltage on the plus (+) terminal must be more positive than the voltage on the minus (–) terminal. The lower voltage limit is therefore zero.

ESR

Real capacitors suffer power-loss during charge and discharge. The loss is caused by resistance in the electrodes, contacts, and in the electrolyte. The standard term for this resistance is Equivalent Series Resistance (ESR). ESR is specified on the data sheet for most commercial capacitors.

One of the simplest models for a real capacitor is ESR in series with an ideal capacitor. The power loss, P_{loss}, during charge or discharge is ESR times the current squared:

$$P_{loss} = I^2 \cdot \text{ESR}$$

This power is lost as heat—under extreme conditions enough heat to damage the device.

Leakage Current

Leakage current is another capacitor non-ideality. An ideal capacitor maintains constant voltage without current flow from an external circuit. Real capacitors require current, called leakage current, to maintain a constant voltage.

Leakage current can be modeled as a resistance in parallel with the capacitor. This model oversimplifies the voltage- and time-dependence of leakage current.

Leakage current discharges a charged capacitor that has no external connections to its terminals. This process is called self-discharge.

Note that a leakage current of 1 μA on a 1 F capacitor held at 2.5 V implies a 2.5 MΩ leakage resistance. The time constant for the self-discharge process on this capacitor is 2.5×10^6 seconds—nearly a month.

Time Effects

The time constant, τ, for charge or discharge of an ideal capacitor in series with ESR is:

$\tau = ESR \cdot C$

Typically τ is between 0.1 and 20 seconds. A voltage step into a capacitor with ESR should create a current that exponentially decays toward zero. In a device with leakage current, the post-step current-decay stops at the leakage current.

Commercial super-capacitors do not show this simple behavior. As seen below, commercial capacitors held at constant potential often take days to reach their specified leakage current. The time needed is much greater than predicted by τ.

One short-term time effect on a capacitor is a phenomenon electrical engineers call *dielectric absorption*. Dielectric absorption is caused by non-electrostatic charge-storage mechanisms with very long time constants.

Time effects may be caused by slow Faradaic reactions occurring at imperfections on the surface of the electrode material. The carbon surfaces used for most super-capacitors have oxygen-containing groups (hydroxyl, carbonyl, and so on) that are plausible reaction sites.

Time effects might also be a side effect of the porosity inherent in high-capacity electrodes. Electrolyte resistance increases with distance into a pore. Different areas of the electrode surface therefore see different resistances. As discussed below, this complicates the simple-capacitor-plus-ESR model into a distributed-element or transmission-line model.

Cycle life

An ideal capacitor can be charged and discharged for an infinite number of cycles. Many commercial super-capacitors approach this idea: they are specified for 10^5 or even 10^6 charge/discharge cycles. Secondary battery cycle-life specifications are typically hundreds of cycles.

The cycle life for all rechargeable devices depends on the exact conditions under which cycling occurs. Currents, voltage limits, device history, and temperature are all important.

Cyclic Voltammetry (CV)

Cyclic Voltammetry (CV) is a widely-used electrochemical technique. Early in a capacitor development project, CV yields basic information about a capacitive electrochemical cell including:

- Voltage window
- Capacitance
- Cycle life

A comprehensive description of CV is well beyond the scope of this application note. Most books describing laboratory electrochemistry have at least one chapter discussing CV.

Description of CV

CV plots the current that flows through an electrochemical cell as the voltage is swept over a voltage range. A linear voltage-ramp is used in the sweep. Often, a CV test repetitively sweeps the voltage between two limit potentials. A pair of sweeps in opposite directions is called a cycle.

Figure 1 presents a CV experiment as a plot of capacitor voltage and current versus time. The darker-colored, saw-toothed waveforms are the voltage applied to the cell; the lighter-colored waveforms are measured current. This graph shows a CV test with three and one-half cycles. Each cycle is shown in a different color.

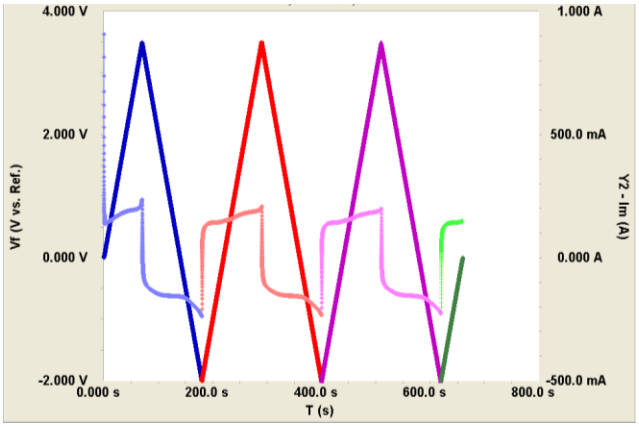

Figure 1. Cyclic Voltammetry as capacitor voltage vs. time. Darker lines are applied voltage; lighter lines are the measured current. Each cycle is a different basic color.

CV may be run with two-electrode or three-electrode cell connections.

Three-electrode connections are common in fundamental research, to allow one electrode to be studied in isolation—without complications from the electrochemistry of the other electrodes. The three electrodes are:

- *Working Electrode*, the electrode being tested.
- *Reference Electrode*, an electrode with a constant electrochemical potential.
- *Counter Electrode*, generally an inert electrode present in the cell to complete the circuit.

Figure 2 shows Gamry's setup for a CV test.

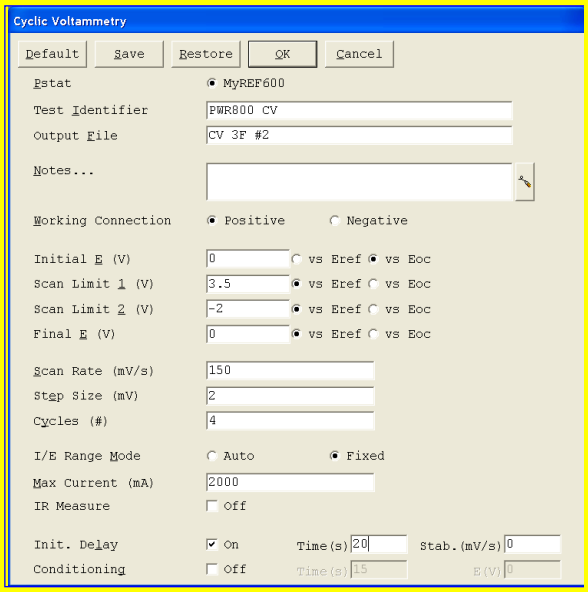

Figure 2. Cyclic Voltammetry set-up window.

Four voltage parameters define Gamry's CV sweep range. The scan starts at the **Initial E**, ramps to **Scan Limit 1**, reverses and goes to **Scan Limit 2**. Additional cycles start and end at **Scan Limit 2**. The scan ends at the **Final E**.

Testing packaged capacitors requires two-electrode connections. All potentiostats can operate with two-electrode connections. Simply connect both the reference electrode and the counter electrode leads to one side of the capacitor. Connect the working electrode lead (and working sense lead, if present) to the other side.

A voltage sweep applied to an ideal capacitor creates a current given by

$$I = \frac{dQ}{dt} = C\frac{dV}{dt}$$

where *I* is current in amperes, and $\frac{dV}{dt}$ is the scan rate of the voltage ramp.

Voltage scan rates for super-capacitor testing are usually between 0.1 mV/s and 1 V/s. Scan rates at the lower end of this range allow slow processes to occur, but take a lot of testing time. Fast scans often show lower capacitance than slower scans. This effect is discussed below.

Be careful: fast scans on high-value capacitors may require more current than the instrument can put out or measure. The maximum allowed scan rate is:

$$\left(\frac{dV}{dT}\right)_{max} = \frac{I_{max}}{C}$$

where I_{max} is the instrument's maximum current in amperes.

Theoretical CV Plot

CV is plotted with current on the *y*-axis and voltage on the *x*-axis. Figure 3 is a theoretical CV plot for a 3 F capacitor in series with a 50 mΩ ESR.

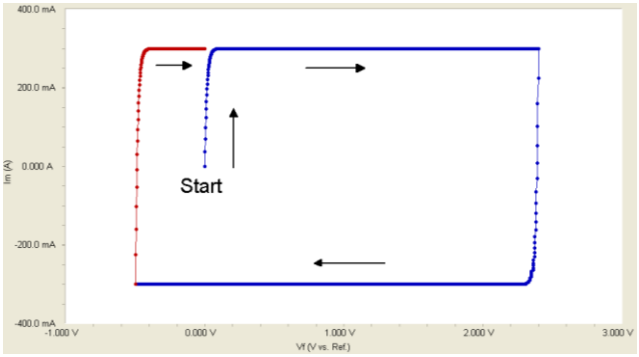

Figure 3. Theoretical cyclic voltammetry for 3 F capacitor in series with a 50 mΩ ESR.

The scan rate is 100 mV/s. The scan limits were:

- Initial E 0.0 V
- Scan Limit 1 2.4 V
- Final E 0.0 V
- Scan Limit 2 –0.5 V

The scan's *Start* is shown on the plot along with arrows showing the direction of the scan. The second cycle is shown in red.

If this CV were recorded on an ideal capacitor (with no ESR), the CV plot would be a rectangle, with height:

$$I = C\frac{dV}{dt} = 300\ \text{mA}$$

ESR causes the slow rise in the current at the scan's start and rounds two corners of the rectangle. The time constant τ, discussed above, controls rounding of corners.

CV on a 3 F EDLC Capacitor

Most of this note's data were recorded using commercial 3 F EDLC capacitors. The parts tested were Nesscap[2] part # ESHSR-0003C0-002R7.

The 100 mV/s cyclic voltammogram of a 3 F capacitor (Figure 4) illustrates how CV can determine a capacitor's voltage window. Notice this plot's similarity to the theoretical CV plot shown above.

[2] Nesscap Energy Inc., 24040 Camino Del Avion #A118, Monarch Beach, CA 92629, USA.

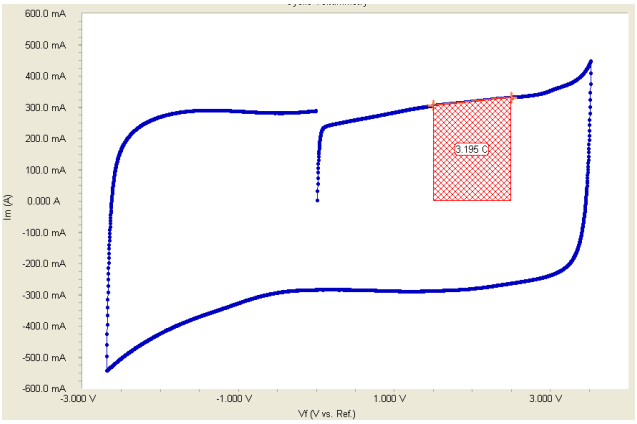

Figure 4. Cyclic voltammogram of 3 F capacitor between +5 V and –3 V, at 100 mV/s. Pink-shaded area is integration of one segment (1.5–2.5 V) of this curve.

The voltage limits entered in Setup were +5 and –3 V. The scan was manually reversed when the current started to increase dramatically. The scan rate was slow enough that a user has time to react to the increased current. The reversal occurred at 3.5 volts, well beyond the 2.7 V specification for this capacitor. The negative going sweep was also manually reversed.

In Gamry's Framework software, selecting `F2-Skip` reverses a sweep.

Integrating a segment of this curve shows calculation of capacitance from CV data. The integrated region (between 1.5 and 2.5 V) is highlighted in pink shading.

Select the integration range using the Echem Analyst's **Select Range Using Keyboard** function.

Integration yielded the charge value shown on the curve. Capacitance is calculated from Q and the voltage range that was integrated:

$$C = \frac{Q}{\Delta V} = \frac{3.195\ \text{C}}{1\ \text{V}} = 3.195\ \text{F}$$

The calculated capacitance depends on the CV scan rate, the voltage region used in the integration, and a myriad of other variables.

Capacitor non-ideality precludes calculation of a true capacitance value for a real-world super-capacitor. Commercial super-capacitors have a specified capacitance value, valid when measured using a specific experiment. Other experimental techniques, including CV, EIS, and many long-term potentiostatic and galvanostatic tests, can give very different capacitance values.

CV Normalized by Scan Rate

A second capacitor was used to show CV's scan-rate dependence. Voltammograms were recorded at scan rates of 3.16, 10, 31.6, 100, and 316 mV/s. The capacitor was held at 0.0 V for 10 min between scans. Scan limits were 0.0 and 2.7 V.

Gamry's **Sequence Wizard** is a convenient tool for setting up complex experiments like this. The zero-volt delay and a CV test were put inside a loop. The scan rate was multiplied by √10 between tests.

A plot of the data obtained from these scans is shown in Figure 5. The purple curve was recorded at the highest scan rate and the red curve at the lowest scan rate.

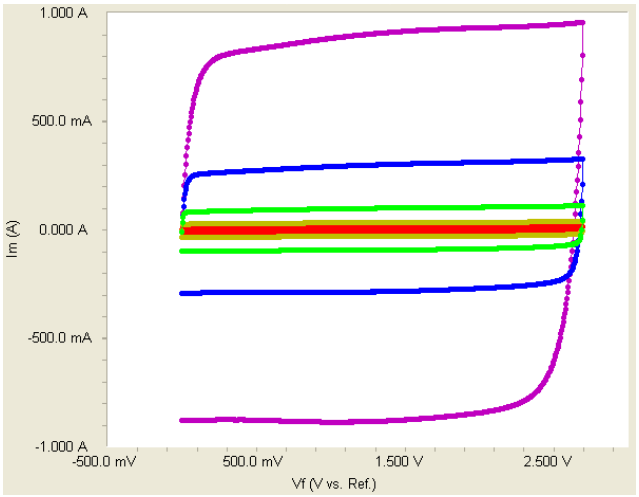

Figure 5. Dependence of cyclic-voltammetry data on scan rate. Purple is fastest; red is slowest.

Figure 6 shows these voltammograms normalized by dividing all currents by the scan rate.

Use the Echem Analyst's CV, **Normalize By Scan Rate** to normalize CV data. Select each curve in overlaid data using the **Curve Selector**  before executing this command. Normalization creates a new curve with `NSR` in the curve's filename.

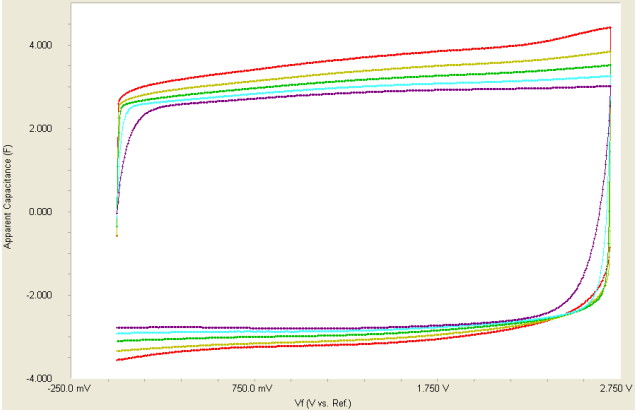

Figure 6. Same CV-data as Figure 4, but normalized to scan rate.

Scan-rate-normalized CV curves of an *ideal* capacitor superimpose: capacitance does not depend on scan rate. After normalization, the *y*-axis units of A·s·volt^{-1} become capacitance in farads.

Super-capacitors are not ideal, so normalized plots do not superimpose. This note calls the *y*-axis of a scan rate normalized CV apparent capacitance, C_{app}.

In Figure 6, C_{app} is ~2.5 F on the curve with the highest scan rate (purple). This curve resembles the CV of an ideal capacitor plus ESR. As scan rate decreases (blue, green, yellow, and red), the C_{app} rises and shows voltage dependence. This is expected for voltage-driven chemical reactions.

C_{app}'s scan-rate dependence can be explained by kinetically slow Faradaic reactions on the electrode surface and by transmission-line behavior caused by electrode porosity. Both cause an increase in C_{app} at lower scan rates.

In the case where slow surface reactions are present, fast scans are over before the reactions occur, so all current is caused by capacitance. Faradaic current has time to flow when scan rates are slower, increasing the total current and C_{app}.

A distributed-element model shows similar scan-rate behavior. Electrode surface that has high electrolyte resistance has no time to respond to voltage changes during a fast scan. In effect, the fraction of electrode surface accessible to the electrolyte depends on the scan rate.

CV to Estimate Cycle Life

CV can also differentiate between poor cycle life and potentially useful cycle life.

Figure 7, the CV plot below, shows 50 cycles between 1.0 and 2.7 V, recorded using a 3 F capacitor. The first, tenth, and fiftieth cycles are shown in blue, green and red.

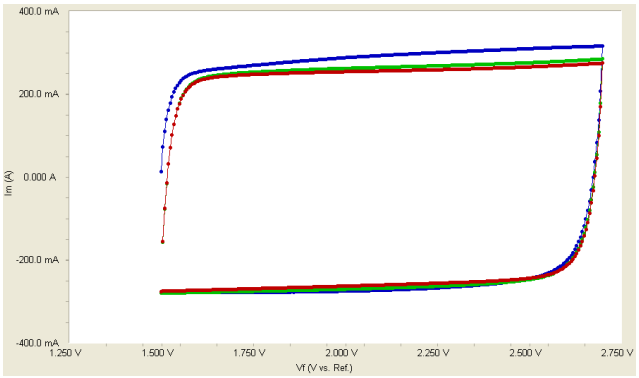

Figure 6. 50 cycles of CV data. Blue = cycle 1; green = cycle 10, and red = cycle 50.

There is very little change in the data between the tenth and the fifieth cycles. Therefore, this capacitor is worthy of cycle-life testing using cyclic charge-discharge techniques (described in Part 2 of this application note).

CV on a Pseudo-capacitor

CV measurements on a pseudo-capacitor differ from the results measured on a true EDLC. We tested a 1 F PAS capacitor from Taiyo Yuden[3] (part number PAS0815LR2R3105). PAS stands for Polyacenic Semiconductor, which is a conductive polymer deposited on the electrodes.

CV tests were run on this device at 3.16, 10, 31.6, 100, and 316 mV/s. The scan range was 0.0 to 2.4 V. The capacitor rested at 0.0 V for 10 min between the scans.

Figure 8 shows the CV curves after normalization by scan rate. The red curve was recorded with the slowest scan rate and purple with the fastest. The *y*-axis is apparent capacitance.

When compared to the normalized CV plot for the EDLC in Figure 6, there is one major difference. The device's C_{app} depends on voltage at all scan rates. This is expected, given the Faradaic nature of charge storage in this pseudo-capacitor.

[3]Taiyo Yuden (U.S.A.) Inc., 10 North Martingale Road, Suite 575, Schaumburg, Illinois 60173, USA.

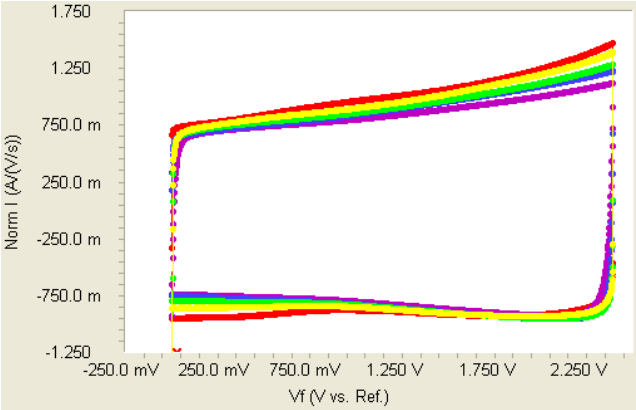

Figure 8. CV for a Taiyo Yuden pseudo-capacitor, normalized to scan rate. Red is the fastest scan rate; purple is the slowest.

Electrochemical Impedance Spectroscopy

Electrochemical Impedance Spectroscopy (EIS) is the preferred method for measuring ESR of super-capacitors. EIS also can measure capacitance and capacitor non-ideality. For basic information on EIS, see Gamry's application note at www.gamry.com:

"Basics of Electrochemical Impedance Spectroscopy"

EIS Model for a Super-capacitor

The most common model fitted to super-capacitor EIS spectra is a simplified Randles model:

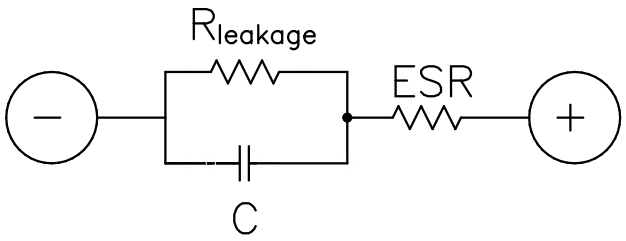

Figure 9. Randles equivalent circuit for modeling super-capacitors.

The elements in the model are

C	Ideal capacitance
ESR	Equivalent Series Resistance
$R_{leakage}$	Leakage resistance

The values used to plot Figure 10 were chosen to approximate those of a typical EDLC device. The EIS magnitude is shown as circles, and the phase is shown as crosses.

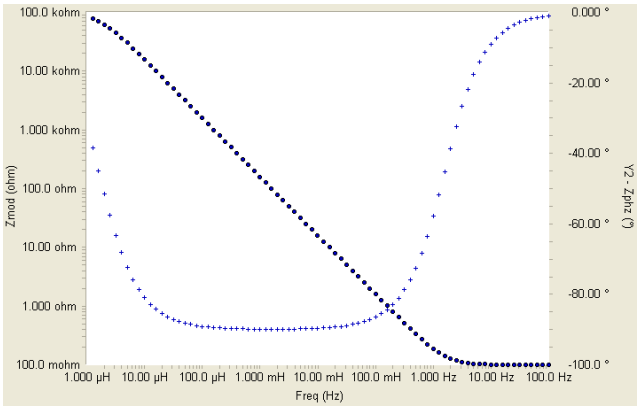

Figure 10. Ideal Bode plot of the equivalent circuit in Figure 8, with C = 1 F, ESR = 100 mΩ, and $R_{leakage}$ = 100 kΩ.

The Bode spectrum in Figure 10 has three regions:

- Above 10 Hz the magnitude and phase approach 100 mΩ and 0°. ESR dominates this region.
- In the region between 100 µHz and 10 Hz, capacitance controls the impedance. Magnitude-versus-frequency is linear (on the log-log Bode plot) with a slope of –1 and the phase approaches –90°.
- Below 10 µHz, the impedance begins a transition back towards resistive behavior as leakage resistance becomes dominant. This transition is incomplete, even at 1 µHz. EIS spectra of real devices rarely give much information about leakage resistance, because its effects are seen at impractically low frequencies.

EIS Measurement Mode

Gamry's EIS300 can measure EIS using three different control modes:

- Potentiostatic EIS
- Galvanostatic EIS
- Hybrid EIS

Potentiostatic and Galvanostatic modes control cell voltage and current respectively. Hybrid mode uses galvanostatic cell control, but changes the AC current to maintain a fixed AC-voltage response.

Galvanostatic and Hybrid mode EIS are preferred for very-low-impedance cells, where small errors in the DC voltage can create huge DC currents.

The impedance of the 3 F capacitors used to generate data for this note is high enough that any mode of control may be used. Potentiostatic mode is the most common EIS mode, so this mode was chosen.

EIS Spectra on a 3 F EDLC at Different Potentials

Figure 11 is a Bode plot of EIS spectra of a 3 F EDLC recorded at three DC potentials: 0.0, 1.25 and 2.50 V (in blue, green and red). The capacitor was held at the DC voltage for 10 min between spectral acquisitions. The spectra were measured potentiostatically with an AC voltage of 1 mV RMS.

The Gamry **Sequence Wizard** was also used to record these data. The loop contained both an equilibration step and EIS data-acquisition.

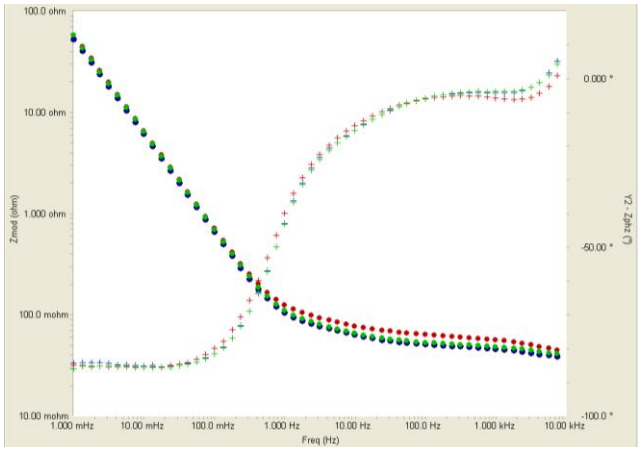

Figure 11. Bode plot of 3 F EDLC at 0.0 V (blue), 1.25 V (green), and 2.50 V (red).

These spectra differ significantly from the ideal in the previous section. Differences include:

- No sign of the leakage resistance in this frequency range.
- Phase between 1 Hz and 100 Hz never approaches the simple model's 0° prediction.

The spectrum of an ideal capacitor is independent of DC voltage. Obviously, the EDLC characterized by these spectra shows non-ideality from 1 Hz to 10 kHz.

Fitting a Model to the Spectrum

The impedance spectrum in Figure 12 was measured on a 3 F EDLC held at 2.25 V. The data were recorded with a 1 mV excitation and potentiostatic cell control. The green lines on this graph are a modified Randles-model fit to the data. The fit parameters are:

C	2.51 F ± 12 mF
ESR	62 mΩ ± 314 μΩ
$R_{leakage}$	773 Ω ± 59 Ω

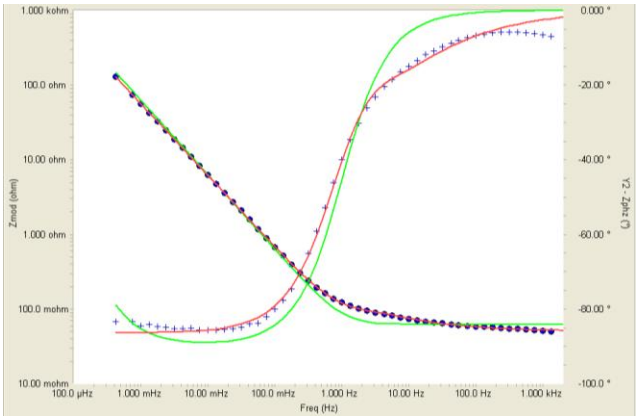

Figure 12. Bode plot of 3 F EDLC at 2.25 V, with Randles model fit (green solid line) and porous-electrode with transmission-line fit (solid red line).

The agreement in Figure 12 between the Randles model and the spectrum is poor. This is typical of EIS on EDLC capacitors where electrode porosity leads to very non-uniform access of the electrolyte to the electrode surface, so Faradaic reactions occur. Simple resistor-and-capacitor models do not apply.

The fit to the data is much better using a porous-electrode, transmission-line model when a Bisquert open element is used (Figure 13).

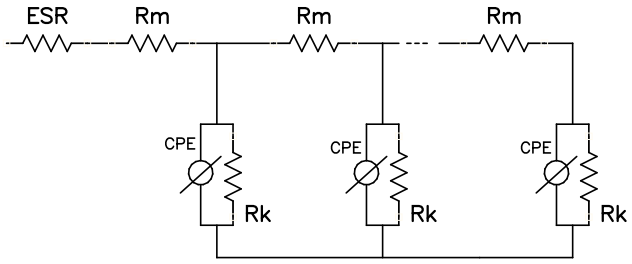

Figure 13. Porous-electrode, transmission-line model used in Figure 12 modeling.

The fit is in red in Figure 11. The fit parameters are:

R_m	112 mΩ ± 22 mΩ
R_k	2.2×10^{30} Ω ± 1×10^{38} Ω
Y_m (CPE)	2.3 S·s/A ± 0.15 S·s/A
α (CPE)	0.960 ± 0.033
ESR	50×10^{-3} Ω ± 639×10^{-6} Ω

For an explanation of the model, see this application note at www.gamry.com:

"Demystifying Transmissions Lines: What are they? Why are they Useful?"

The high uncertainty in R_k is expected. The spectrum does not include frequencies where R_k affects the impedance.

EIS Spectrum of a Low-ESR 650 F EDLC

EIS measurement on very-low-ESR capacitors is difficult. It generally requires:

- True four-terminal measurements
- Galvanostatic cell control
- Low-resistance contacts
- Twisted-pair or coaxial cell leads

Two of Gamry's application notes give suggestions for making low-impedance EIS measurements:

"Accuracy of Contour Plots"

"Verification of Low-impedance EIS Using a 1 mΩ Resistor"

EIS spectra were recorded on a Maxwell[4] capacitor (part number BCAP0650 P270). This 650 F capacitor was rated for ESR less than 600 μΩ at 1 kHz.

Figure 14 is a photograph that shows the connections used to record the EIS spectrum of this device. Connections were made with 1.5 mm-thick copper sheet. The current-carrying leads and voltage-sensing leads are on opposite sides of the device.

Figure 14. Connections from the potentiostat to the Maxwell capacitor.

Warning: Avoid shorting capacitor terminals though low-resistance connections. Very dangerous currents of hundreds or even thousands of ampères could flow.

The EIS spectrum is presented in Figure 15. This spectrum was recorded in Hybrid Mode with a 1 mV AC voltage. The impedance at 1 kHz is 335 μΩ, which is less than this capacitor's rated ESR of 600 μΩ.

[4]Maxwell Technologies, Inc., 3888 Calle Fortunada, San Diego, CA 92123.

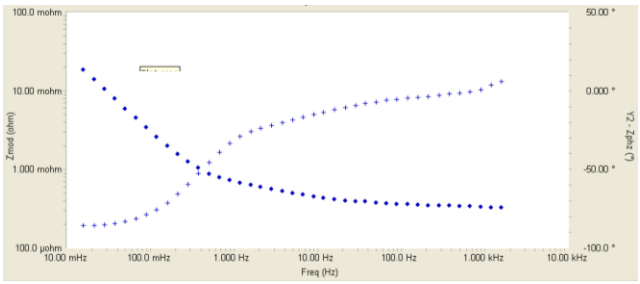

Figure 15. EIS from 650 F EDLC.

EIS on a Pseudo-capacitor

EIS spectra recorded on an ideal capacitor at different DC voltages should superimpose.

EIS confirms the voltage dependence of measured capacitance on a PAS pseudo-capacitor. This is the same capacitor used previously for CV testing. EIS spectra were recorded at DC voltages of 0, 1.2, and 2.4 V (Figure 16). Unlike the EDLC case, low-frequency impedance was different at each voltage.

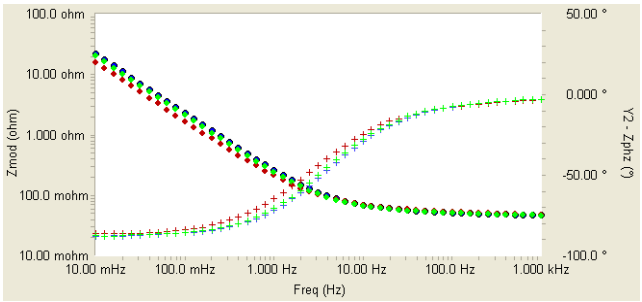

Figure 16. EIS for a PAS pseudo-capacitor at 0 (blue), 1.2 (green), and 2.4 V (red).

In the simple Randles model, capacitance controls the impedance at the lowest frequencies in the graph above. In the plot above, impedance in this region depends on DC voltage, so the capacitance must also depend on DC voltage.

Measurement of Leakage Current

Leakage current can be measured in at least two ways:

- Apply a DC voltage to a capacitor and measure the current required to maintain that voltage.
- Charge a capacitor to a fixed voltage, then open the circuit on the capacitor and measure the voltage change during self-discharge.

Conway's book includes a chapter that discusses leakage current and self-discharge of super-capacitors.

In an attempt to make the specifications of a super-capacitor look good, some manufacturers specify that leakage current is measured after 72 hours with voltage

applied. Under these conditions, leakage current can be as low as 1 μA/F.

Direct Measurement of Leakage Current

Direct potentiostatic measurement of capacitor leakage current is quite challenging. The test must apply a DC potential to capacitor under test, and measure extremely small currents.

Typically, capacitor charging currents are in ampères and leakage currents are in microampères, a range of 10^6. Noise or drift in the DC potential can create currents that are larger than the leakage current.

For example, assume the 3 F capacitors used in our testing have an ESR of 100 mΩ. We want to measure a leakage current of 1 μA on these: we'd like current noise to be less than the 1 μA signal.

At frequencies where ESR is the dominant impedance, 0.1 μV of noise in the applied voltage will create a noise current of 1.0 μA. At lower frequencies, where our 3 F capacitance dominates the impedance, a voltage drift of 0.3 μV/s creates a current of 1.0 μA.

Fast acquisition of data, external noise sources, or lack of a Faraday cage can lead to large apparent DC currents or continual switching between current ranges.

The Potentiostatic test in Gamry's PWR800 Electrochemical Energy Software *will not* accurately measure leakage current, for it only offers a dynamic range of about 10^4.

PWR800 Leakage-current Measurement

Figure 17 presents leakage current measured on a new 3 F capacitor. The plot is logarithm of current versus time for five days at 2.5 V.

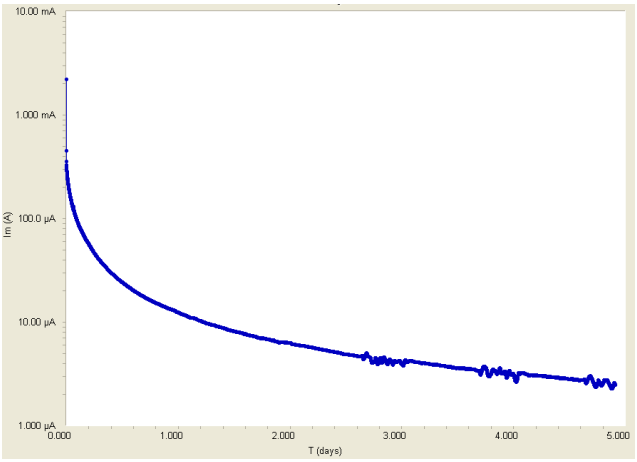

Figure 17 Leakage current vs. time for a 3 F capacitor.

Note that current is still falling five days after application of the potential. The manufacturer specifies leakage current on this capacitor at less than 5 μA after 72 hours; the measured value was about 3.2 μA.

The data in this plot were smoothed using a Savitsky-Golay algorithm with a 60 s window. The periodic noise signal is caused by daytime air-conditioning.

A special script has been developed for direct leakage-current measurement using the PWR800 tools. This script is named:

`PWRLeakageCurrent.exp`

Unlike the PWR800 potentiostatic technique, this script applies a voltage using the instrument's potentiostat mode and measures leakage current.

It uses a user-entered estimate for ESR to avoid I/E Converter ranges where voltage noise can overload the current measurement circuitry. A gain of 10 in the current measurement allows measurement with ten times greater voltage noise and drift.

Measurement of Self-discharge

Self-discharge causes the open-circuit voltage of a charged capacitor to decrease over time. During self-discharge, leakage current discharges the capacitor, even though there is no external electrical current.

Conway's book describes three mechanisms for self-discharge. These mechanisms can be distinguished by analyzing the shapes in voltage-versus-time curves recorded over long periods of time. This analysis was not done on the data presented here.

Instantaneous leakage current, I_{leak}, can be calculated by multiplying the rate of voltage-change during self-discharge by capacitance.

$$I_{\text{leak}} = C\frac{dV}{dt}$$

The graph ion Figure 18 is the open-circuit voltage-versus-time curve of a 3 F capacitor left open-circuit after 12 hours at 2.5 V. This was recorded with the capacitor pre-charged to 2.5 V in the previous test. The voltage change was less than 2 mV after 30 min.

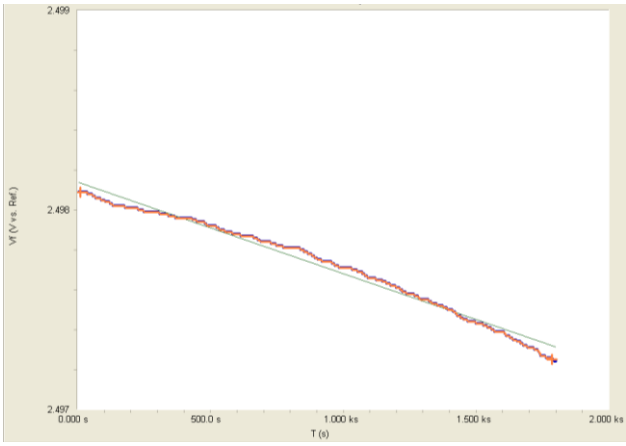

Figure 18. Voltage-decay with time of a 3 F capacitor, after 12 h charge to 2.5 V.

The red line on the graph is a linear-least-squares fit of the voltage-decay data. The slope is 0.55 μV/s.

The leakage current is

$$I_{\text{leak}} = C\frac{dV}{dt} = 3\ \text{F} \cdot \frac{0.55\ \mu\text{V}}{\text{s}} = 1.6\ \mu\text{A}$$

The slope calculation used the **Linear Fit** function in Gamry's Echem Analyst.

The PWR800 has added a script that makes this measurement. This script is named:

`PWR_SelfDischarge.exp`

It applies a constant potential for a user-requested length of time. It then turns off the cell and measures changes in open-circuit voltage. The instrument's offset and gain circuitry allows measurement of very small voltage-differences.

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