ApplicationNOTE

GAMRY INSTRUMENTS

Testing Electrochemical Capacitors
Part 3 – Electrochemical Impedance Spectroscopy

Purpose of This Note

This application note is the third part of notes describing electrochemical techniques for energy storage devices. This note discusses basics of Electrochemical Impedance Spectroscopy (EIS) and introduces Gamry's EIS techniques by measurements on single electrochemical capacitors (ECs) and stacks.

Introduction

Part 1 of this series of notes discusses theoretical basics of capacitors and describes several techniques to investigate electrochemical capacitors.

Part 2 explains Gamry's Electrochemical Energy PWR800 software for cycling of energy storage devices. Effects of different parameters during cycling of single cells and stacks are described.

All parts of this note can be found in the Application Notes section of Gamry's website: www.gamry.com.

Experimental

This note describes several EIS techniques that can be performed with Gamry's Framework. For this purpose, measurements were done on 3 F electric double layer capacitors (EDLCs) (P/N ESHSR-0003C0-002R7) and 5 F EDLCs (P/N ESHSR-0005C0-002R7) from Nesscap, a 650 F EDLC (P/N BCAP0650 P270) from Maxwell, and a 1 F PAS pseudocapacitor (P/N PAS0815LR2R3105) from Taiyo Yuden. The acronym PAS stands for polyacenic semiconductor which is a conductive polymer deposited on the electrodes.

The data in this note were recorded using Gamry's EIS300 software and a Reference 3000. All plots were generated and evaluated using Gamry's Echem Analyst.

Electrochemical Impedance Spectroscopy

Electrochemical Impedance Spectroscopy is a widely used technique to investigate electrochemical systems. The advantage of EIS is that it is generally non-destructive to the investigated system. This enables the possibility for further electrochemical measurements and post-mortem investigations.

EIS is the most common method for measuring the equivalent series resistance (ESR) of ECs. It also allows creating models to describe underlying reaction mechanisms. With these models capacitor non-idealities can be investigated.

Generally, a sinusoidal AC excitation signal is applied to the investigated system during an EIS experiment and the AC response is measured. The frequency of the input signal is varied during the measurement. Finally, the impedance Z of the system is calculated, expressed in terms of magnitude Z_0 in ohms (Ω) and phase shift ϕ in degree (°).

If you need basic information on EIS, see Gamry's application note at **www.gamry.com**:

Basics of Electrochemical Impedance Spectroscopy

EIS measurement modes

Gamry's EIS300 software can measure impedance spectra using four different modes:

- Potentiostatic
- Galvanostatic
- Hybrid
- OptiEIS

In potentiostatic mode a DC voltage is applied that is superimposed by an AC voltage signal. The frequency of the signal is changed during the experiment and the phase sensitive AC current response is measured.

Galvanostatic mode is similar to potentiostatic mode. In contrast, a DC current superimposed by an AC current signal is applied to the system and the phase sensitive AC voltage response is measured.

Hybrid EIS also uses galvanostatic cell control. In addition, the amplitude of the AC current is adjusted to maintain a nearly constant AC potential response.

Potentiostatic mode is most common in research. However, small errors in the applied DC voltage can lead to huge DC currents in low-impedance cells destroying the cell. Hence, galvanostatic and Hybrid EIS are preferred for low-impedance cells.

Three application notes give suggestions for making low-impedance EIS measurements. They can be found at Gamry's website **www.gamry.com**:

Accuracy Contour Plots

Verification of Low Impedance EIS Using a 1 mΩ Resistor

Low Impedance EIS at its Limits with the Reference 30k Booster

OptiEIS is a multisine technique and differs from the other methods described above. Instead of a single sinusoidal waveform with only one frequency, multiple waveforms with several frequencies are applied to the system at the same time. Hence the length of EIS measurements can be reduced by up to a factor of four. OptiEIS can be run potentiostatically or galvanostatically.

For more information on multisine EIS, see Gamry's application note at **www.gamry.com**:

OptiEIS: A Multisine Implementation

Randle's model for electrochemical capacitors

The ideal capacitor does not exist. In reality, several effects lead to imperfections in the system. Hence, different models are used to describe the investigated system.

The most common and simplest model fitted to EIS spectra of electrochemical capacitors is a simplified Randle's model, shown in Figure 1:

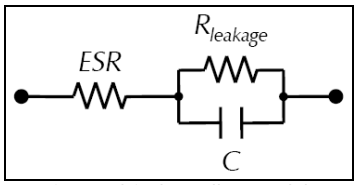

Figure 1 – Diagram of a simplified Randle's model.

The circuit elements in the model are:

- ESR Equivalent series resistance
- $R_{leakage}$ Leakage resistance
- C Ideal capacitance

The ESR is modeled in series to the ideal capacitance. Resistances from the electrolyte, the electrodes, and electrical contacts are summarized in the ESR. A small ESR leads to better performances of energy storage devices.

In contrast, a small leakage resistance $R_{leakage}$ leads to a higher leakage current which is responsible for self-discharge of a charged capacitor when no external load is connected. The leakage resistance is modeled parallel to C.

Figure 2 shows a Bode plot of Randle's model in the frequency range between 10 kHz and 1 μHz. The fit-parameters are typical values for electrochemical capacitors:

- ESR 100 mΩ
- $R_{leakage}$ 100 kΩ
- C 1 F

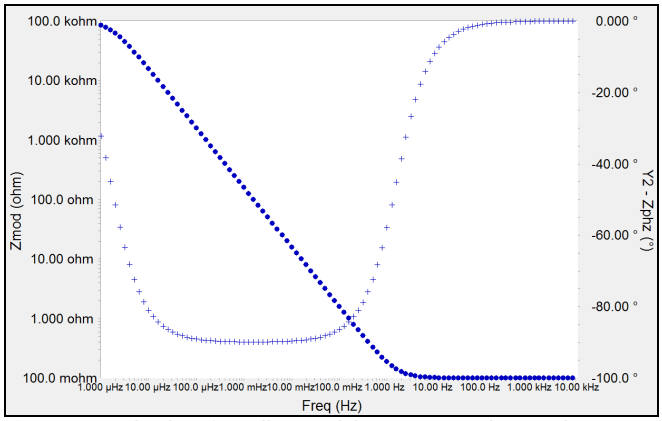

Figure 2 – Bode plot of Randle's model. (●) magnitude, (+) phase.

The Bode spectrum of a typical Randle's model has three regions:

- Above 10 Hz, magnitude and phase approach 100 mΩ and 0° respectively. The ESR dominates this region.
- Between 100 μHz and 100 mHz, capacitance controls the impedance. Magnitude versus frequency is linear (on the log-log Bode plot) with a slope of -1 and the phase approaches -90°.
- Below 10 μHz, the impedance begins a transition back towards resistive behavior as leakage resistance becomes dominant. This transition is incomplete even at 1 μHz.

EIS spectra of real devices rarely give much information about leakage resistance because its effects are seen at impractically low frequencies. Measurements at these frequencies take up a lot of time.

Part 1 of this application note series describes in detail methods to measure leakage current.

Transmission line models for electrochemical capacitors

Real electrochemical capacitors do not show the simple behavior of Randle's model.

Figure 3 shows a Bode plot of a 3 F EDLC. In addition, two different models are shown – the simplified Randle's model (red curve) and the Bisquert open model (green curve).

The impedance of the 3 F EDLCs used to generate data for this note is high enough that any control mode can be used. As potentiostatic EIS is most common, this mode was used.

The capacitor was first charged to 2.7 V and held at this potential for 10 minutes. For the EIS experiment, DC voltage was set to 2.7 V superimposed by an AC voltage of 1 mV. The frequency ranged from 10 kHz to 100 μHz.

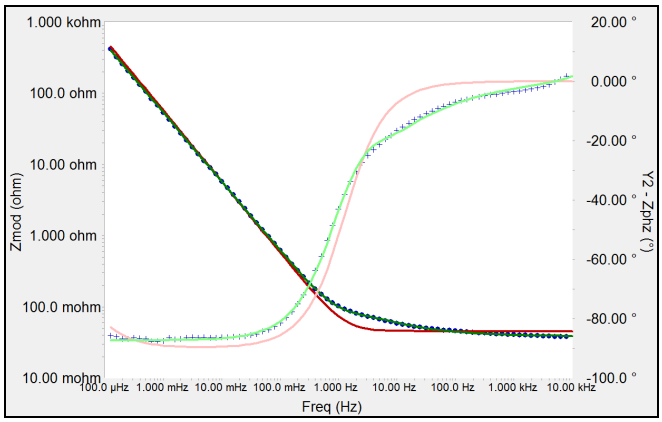

Figure 3 – Bode diagram of a potentiostatic EIS test on a 3 F EDLC (●). (●) Randle's model, (●) Bisquert open model. (●) magnitude, (+) phase. For details, see text.

As expected, fitting Randle's model to the spectrum shows poor agreement. The fit-results are:

- ESR 45.5 mΩ ± 0.2 mΩ
- $R_{leakage}$ 3.6 kΩ ± 0.4 kΩ
- C 2.75 F ± 0.01 F

This result is typical for EIS spectra of electrochemical capacitors where electrode porosity leads to very non-uniform electrolyte access to the electrode surface and Faradaic reactions occur. Simple resistor and capacitor models do not apply.

Differences between Randle's model and real ECs include:

- Between 10 Hz and 10 kHz, magnitude is not constant but slightly increasing. The transition from resistive to capacitive behavior occurs in stages.
- Phase never approaches the simple model's 0° prediction at higher frequencies.
- No sign of leakage resistance is seen in this frequency range.

The fit to the data is much better using a porous electrode transmission line model. Figure 4 shows the Bisquert open model that describes also electrode porosity.

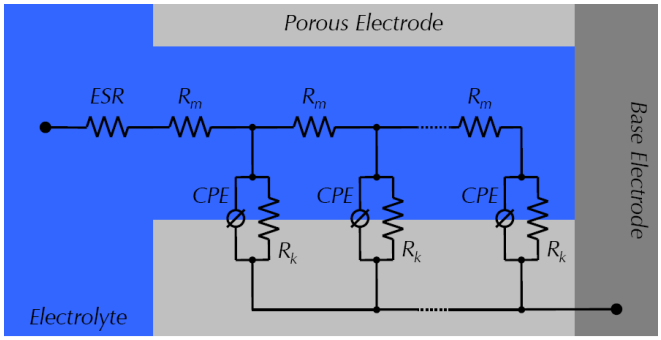

Figure 4 – Diagram of the Bisquert open model.

Among ESR, a pore resistance R_m is added that increases with increasing pore depth. A constant phase element (CPE) replaces the ideal capacitance and defines inhomogeneities of the electrode surface in ECs. An interfacial resistance R_k similar to the leakage resistance is parallel to CPE and completes the model.

For more information on transmission line models, see Gamry's application note at **www.gamry.com**:

Demystifying Transmission Lines: What Are They, Why Are They Useful?

The fit of the Bisquert open model in Figure 3 is colored green. The fit-parameters are:

- ESR 38.2 mΩ ± 0.4 mΩ
- R_m 96 mΩ ± 17 mΩ
- R_k $1.3 \cdot 10^{34}$ Ω ± $1 \cdot 10^{38}$ Ω
- Y_m (CPE) 2.54 S·s$^{\alpha}$ ± 0.15 S·s$^{\alpha}$
- α (CPE) 0.97 ± 0.03

The Bisquert open model complies much better with the Bode plot in Figure 3 than Randle's model and overlaps nearly complete.

Transmission line models take into account the stepwise increase of the magnitude at higher frequencies. The transition region from resistive to capacitive behavior at frequencies above 100 mHz is described much better. Hence the fit-value for the ESR is smaller than the result of Randle's model.

The high uncertainty in the interfacial resistance R_k is expected. This resistance dominates the impedance in the low-frequency region that is not included in the spectrum.

EIS on a 3 F EDLC at different potentials

For ideal EDLCs, EIS spectra are independent of the applied DC voltage. However, real devices do not show this tendency.

Figure 5 shows Bode plots of a 3 F EDLC recorded at five different DC potentials: 0 V, 1 V, 2 V, 3 V, and 3.5 V.

The last value is way above the 2.7 V specification of the EDLC.

The spectra were measured potentiostatically with an AC voltage of 1 mV_{rms} in a frequency range from 10 kHz to 10 mHz. The capacitor was held at the DC voltage for 10 minutes before each measurement.

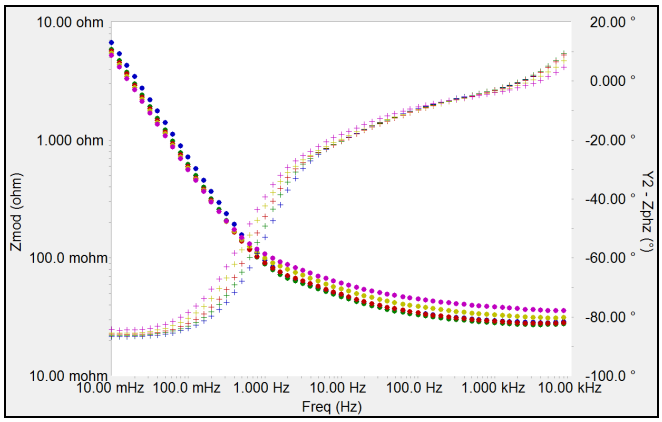

Figure 5 – Bode diagrams of potentiostatic EIS tests on a 3 F EDLC. (●) 0 V, (●) 1 V, (●) 2 V, (●) 3 V, (●) 3.5 V. (●) magnitude, (+) phase. For details, see text.

Obviously, this EDLC shows non-ideality between 1 Hz and 10 kHz. Exceeding the rated voltage of the capacitor can cause decomposition and deposition reactions on the electrode surface. These irreversible Faradaic reactions can lead to an increase in ESR shown in the frequency range above 1 Hz where ESR dominates the impedance.

Below 1 Hz, impedance is decreasing with increasing voltage. In this frequency region impedance depends on the DC voltage, so the capacitance increases and must also depend on DC voltage. Note that increased capacitances at higher potentials can be at the cost of shorter life-times.

EIS on a 1 F pseudocapacitor at different potentials

Just as for ideal EDLCs, EIS spectra recorded on an ideal pseudocapacitor should superimpose at different DC voltages. Also for real pseudocapacitors this behavior does not apply.

Figure 6 shows Bode plots of a 1 F PAS pseudocapacitor recorded by potentiostatic EIS mode. The DC voltages were 0 V, 1 V, 2 V, and 2.4 V. The AC voltage was set to 1 mV_{rms}. The frequency range was between 10 kHz and 10 mHz.

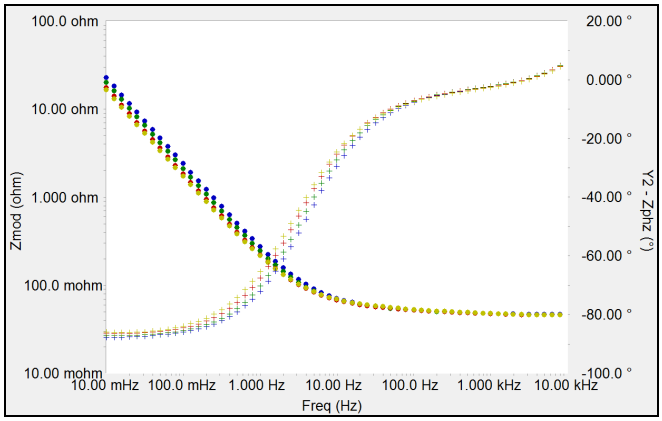

Figure 6 – Bode diagrams of potentiostatic EIS tests on a 1 F PAS pseudocapacitor. (●) 0 V, (●) 1 V, (●) 2 V, (●) 2.4 V. (●) magnitude, (+) phase. For details, see text.

Just as EDLCs, pseudocapacitors show voltage dependence in impedance at lower frequencies. With increasing voltage impedance decreases.

In contrast to the 3 F EDLC (see Figure 5), this 1 F pseudocapacitor showed no voltage dependence at frequencies above 10 Hz.

EIS on a low-ESR 650 F EDLC

EIS measurements on low-ESR capacitors are difficult. It generally requires:

- True 4-terminal measurements
- Galvanostatic cell control
- Low-resistance contacts
- Twisted pair or coaxial cell leads

Figure 7 shows the connections used to record the EIS spectrum of a 650 F EDLC. 1.5 mm thick copper sheets were used for the connections. Note that the current carrying leads (green and red) and the voltage sensing leads (white and blue) are on opposite sides of the device.

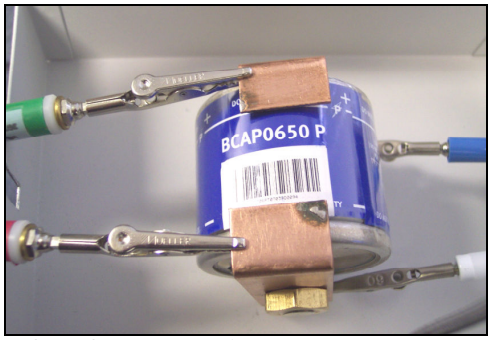

Figure 7 – Electrode connections for measurements on a 650 F EDLC. Working (green), Counter (red), Working sense (blue), and Reference (white).

Caution: You need to be very careful to avoid shorting capacitor terminals though low-resistance connections. Very dangerous currents of hundreds or even thousands of amps could flow.

As mentioned above, galvanostatic mode is necessary for low-impedance cells. Using potentiostatic mode, small errors in DC voltage can lead to high currents destroying the cell or exceeding the potentiostat's specifications.

Figure 8 shows a Hybrid EIS spectrum of a 650 F EDLC. The capacitor was first charged to 2 V and held at this potential for 30 minutes to maintain a constant voltage during the EIS measurement. The DC current was zero and the AC voltage was 0.1 mV_{rms}. The EIS spectrum was recorded from 1 kHz to 10 mHz.

Note that Hybrid EIS is still working in galvanostatic mode although an AC voltage is defined in the setup. The galvanostat modifies the AC current to maintain nearly the adjusted AC voltage response.

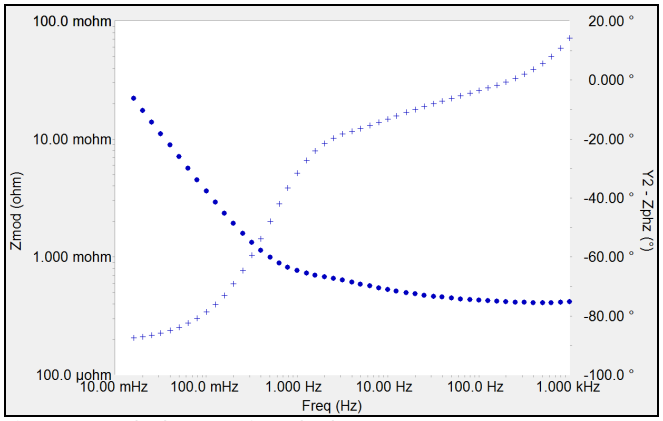

Figure 8 – Bode diagram of a Hybrid EIS test on a 650 F EDLC. (●) magnitude, (+) phase. For details, see text.

This 650 F EDLC has a rated ESR of less than 600 µΩ at 1 kHz. The measurement yields a value of 418 µΩ which is less than this capacitor's rated ESR of 600 µΩ.

Looking at the DC potential of the EDLC during the EIS measurement, it changes only by about 2 mV which is necessary for reliable results.

OptiEIS – a multisine technique

Gamry's OptiEIS enables the user the possibility to perform EIS measurements faster than with conventional single-sine techniques.

Figure 9 shows Bode plots of a potentiostatic EIS test and an OptiEIS experiment in potentiostatic mode on a 3 F EDLC. The capacitor was first charged to 2.7 V and held at this potential for 20 minutes. A DC voltage of 2.7 V and an AC voltage of 10 mV were applied. The frequency ranged from 40 Hz to 10 mHz.

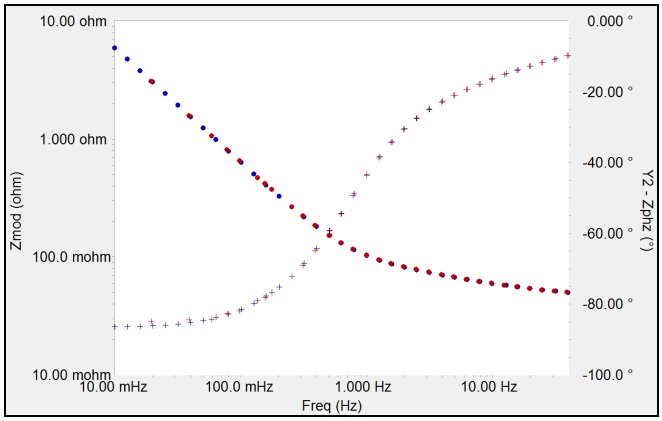

Figure 9 – Bode diagrams of a potentiostatic EIS test (●) and an OptiEIS test (●) on a 3 F EDLC. (●) magnitude, (+) phase. For details, see text.

Both Bode plots of the potentiostatic EIS and OptiEIS experiments overlap perfectly. In low noise mode, the potentiostatic EIS test takes about 30 minutes. With OptiEIS, measurement time is reduced to only 9 minutes which is a factor of about three.

EIS during cycling experiments

EIS can be combined with other techniques, e.g. cyclic charge discharge (CCD) tests. This combination enables investigation of changes in a system with time.

For detailed information about practical applications and evaluation of CCD tests see part 2 of this application note series.

Figure 10 shows the changes of capacity during a CCD experiment. Ten sequences were run, each had 5,000 cycles. Prior to the first cycle and after each sequence a galvanostatic EIS experiment was performed. The total number of cycles was 50,000.

For the CCD test a 3 F EDLC was first charged to 1.35 V and then cycled between 1.35 V and 3.5 V with a current of ±2.25 A.

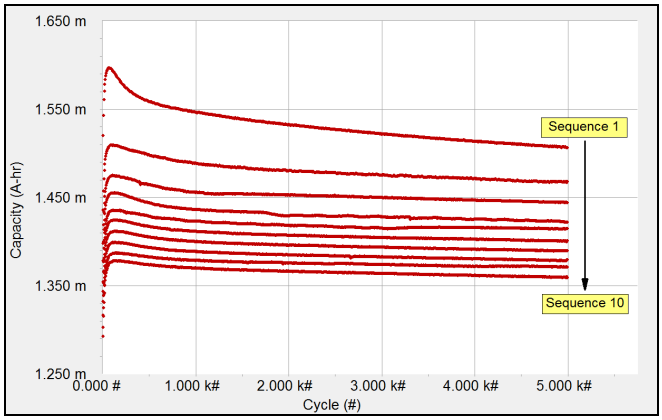

Figure 10 – CCD test on a 3 F EDLC over 50,000 cycles interrupted by galvanostatic EIS experiments. For details, see text.

To perform complex sequences, Gamry offers the ***Sequence Wizard***. It allows building of individual sequences with a wide spectrum of techniques.

For more information about the *Sequence Wizard*, visit Gamry's website **www.gamry.com**.

Capacity decreases with increasing cycle number. As the upper voltage limit of 3.5 V is way above the limitations of the EDLC, irreversible reactions on the electrode surface can occur which decrease the performance.

Figure 11 shows the Bode plots. Zero DC current and 10 mA_{rms} AC current were applied. The spectra were recorded from 10 kHz to 100 mHz. Prior to each EIS test, the potential was held at 3.5 V for four hours.

Important Note: The hold step is necessary, keeping the system in steady state during the galvanostatic EIS measurement, to fulfill the stability criterion for EIS.

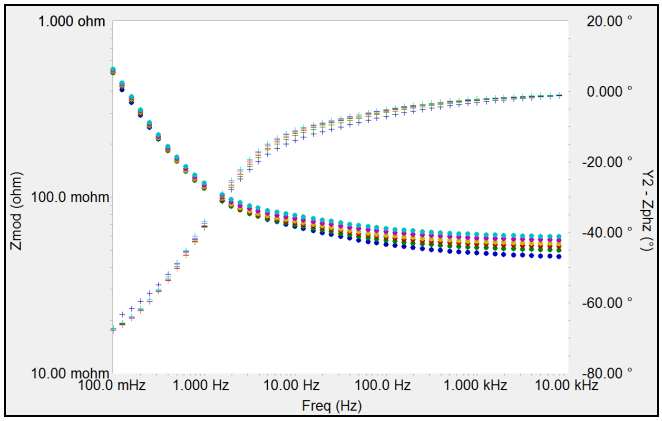

Figure 11 – Bode diagrams of galvanostatic EIS tests on a 3 F EDLC during cycling. (●) 1st cycle, (●) 10,000th cycle, (●) 20,000th cycle, (●) 30,000th cycle, (●) 40,000th cycle, (●) 50,000th cycle. (●) magnitude, (+) phase. For details, see text.

Impedance increases in the frequency range between 1 Hz and 10 kHz with increasing cycle number. In this region ESR dominates the impedance. Evaluation of the fits for these spectra confirms that the ESR increases. After 50,000 cycles the ESR increased by about 14 mΩ. That corresponds to an increase of more than 30 %.

In contrast, capacitance decreases with increasing cycle number due to irreversible reactions that can occur on the electrode surface.

Table 1 lists the fit-values for the ESR and capacitance dependent on the cycle number.

Cycle #	1	10k	20k	30k	40k	50k
ESR [mΩ]	44.5	48.7	51.4	53.1	55.8	58.4
C [F]	3.01	2.94	2.90	2.87	2.84	2.81

Table 1 – Change of ESR and capacitance dependent on cycle number.

EIS on stacks

Stacks of single energy storage devices are used for high-voltage applications. For this, cells are connected in serial and parallel circuits.

For further information about cell stacks see part 2 of this application note series.

Figure 12 shows a test setup for stack measurements used in this note. It consists of a serial connection of two 3 F EDLCs and one 5 F EDLC. A higher ESR is simulated for the second capacitor with a 0.5 Ω resistor in series.

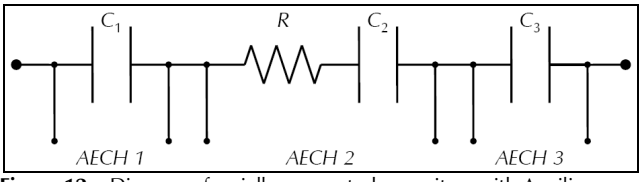

Figure 12 – Diagram of serially connected capacitors with Auxiliary Electrometer connections (AECH 1, AECH 2, and AECH 3). The serial resistor *R* simulates a higher ESR.

The voltage of each single cell was measured with individual channels of Gamry's ***Auxiliary Electrometer***.

The ***Auxiliary Electrometer*** is currently supported in PWR800, EIS300, and the DC and AC Toolkits.

For more information on the Auxiliary Electrometer option, visit Gamry's website **www.gamry.com**.

For the EIS experiments with a stack, every single cell was initially charged to 1 V. After this, the stack was charged to 9 V with a current of 3 A. The potential was held for 20 minutes prior to the EIS measurement.

Figure 13 shows Bode plots of the stack and all three single cells that were recorded simultaneously with the Auxiliary Electrometer. The EIS experiment was performed in galvanostatic mode with zero DC current and 10 mA_{rms} AC current. The frequency ranged from 10 kHz to 1 mHz.

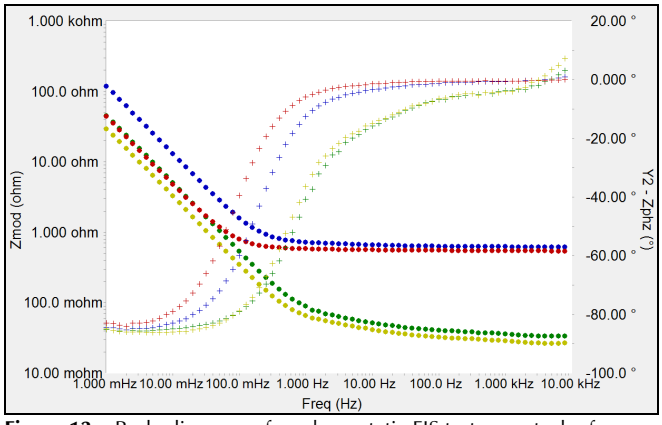

Figure 13 – Bode diagrams of a galvanostatic EIS test on a stack of EDLCs. (●) stack, (●) C_1, (●) C_2 + R, (●) C_3. (●) magnitude, (+) phase. For details, see text.

At frequencies above 1 Hz, differences in ESR of each single cell can be seen. As the total voltage *U* of the stack, also the total ESR is the sum of the parameters of each single cell. Hence spectra are shifted upwards above 1 Hz with increasing ESR.

In contrast, the total capacitance *C* of a stack is the inverse of the sum of the reciprocal single capacitances. Hence total *C* is lower than the single capacitances. Below 100 mHz, in the linear region of the magnitude, spectra are shifted towards the bottom left corner of the diagram with increasing capacitance.

Table 2 summarizes some parameters of the investigated stack and its single cells. ESR and capacitance *C* were calculated by fits from each EIS spectrum. The potential *U* was recorded during the charge step.

Element	*U* [V]	ESR [mΩ]	*C* [F]
Stack	9.00	613	1.27
C_1	2.78	35.7	3.28
C_2 + *R*	3.55	543	3.49
C_3	2.67	31.2	5.01

Table 2 – Measured parameters of the stack and its single cells.

Looking only at the parameters of the stack does not reveal imbalances of single cells. For example, if the stack would be perfectly balanced and charged to 9 V, all single capacitors would be evenly charged to 3 V.

Due to unbalanced cell parameters (e.g. different ESR and different capacitances), the charge potentials of the single cells are varying. Note that these differences can not be seen in the total stack voltage which is still 9 V.

As capacitor C_2 has the highest simulated ESR, it overcharged by more than 0.5 V whereas C_1 and C_3 did not reach the desired potential. Overcharging can damage a cell and drastically reduce performance and life-time.

By using the Auxiliary Electrometer, the whole stack and each single cell can be investigated simultaneously. In this way, imbalances in capacitances, ESR, and cell potentials can be observed. The stack can be balanced by adjusting these parameters.

Conclusion

This application note discussed theory and practice of EIS measurements with electrochemical capacitors. It showed that EIS is an indispensable tool to investigate energy storage devices.

Two models were explained to fit Bode spectra of ECs. However, for reliable fitting results models are necessary that describe the porosity of high-surface electrodes used in ECs, so-called transmission line models.

Based on several measurements on ECs different techniques were described: Potentiostatic EIS, galvanostatic EIS, Hybrid EIS, and Gamry's multisine technique OptiEIS.

To show the wide field of application of EIS, CCD tests were combined with EIS measurements to monitor changes in the system during time.

Finally, stack measurements were performed by means of Gamry's Auxiliary Electrometer. In this way, single cells of a stack can be investigated simultaneously for balancing individual cell parameters.

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734 Louis Drive • Warminster, PA 18974, USA • Tel. 215 682-9330 • Fax 215 682-9331 • www.gamry.com • info@gamry.com