ApplicationNOTE

GAMRY INSTRUMENTS

Testing Electrochemical Capacitors
Part 1 – Cyclic Voltammetry and Leakage Current

Purpose of This Note

This application note is the first part of an overview of electrochemical techniques used to test electrochemical capacitors (ECs). Commercially available electrochemical capacitors were tested to explain and discuss the theoretical background of cyclic voltammetry and leakage current measurement.

Introduction

Part 2 of this note discusses techniques that are also familiar to battery technologists. Part 3 describes theory and practice of EIS measurements on capacitors.

All parts can be found in the Application Notes section on Gamry's homepage: www.gamry.com.

In contrast to batteries, ECs generally store energy by highly reversible separation of electrical charge while batteries use chemical reactions.

ECs consist of two high-surface electrodes immersed in a conductive liquid or polymer called the electrolyte. The electrodes are separated by an ionic-conducting separator that prevents shorts.

Compared to a battery, an electrochemical capacitor has the following advantages:

- Higher charge and discharge rates (high power density)
- Longer cycle-life (> 100,000 cycles)
- Low toxicity materials
- Operation over a wide temperature range
- Low cost per cycle

These are offset by some disadvantages:

- Higher self-discharge rate
- Lower energy density
- Lower cell voltage
- Poor voltage regulation
- High initial cost

Some applications use electrochemical capacitors in parallel with a battery. This combination provides better cycle-life and higher power than a battery alone.

State of the art applications for electrochemical capacitors include:

- Hybrid Electric Vehicles (HEVs)
- Diesel engine starting systems
- Cordless power tools
- Emergency and safety systems

For more information read Brian Conway's book on electrochemical capacitor technology:

Conway, B. E., *Electrochemical Supercapacitors: Scientific Fundamentals and Technological Applications*, Kluwer Academic Press / Plenum Publishers, New York, NY, 1999.

Similar Technology – Confusing Names

In technical papers and for commercial products a variety of terms is used to define types of capacitors. Unfortunately, arbitrariness leads to confusion and misleading designations.

These names are mostly product names and often used incorrectly. A selection is listed below:

- Supercapacitors
- Ultracapacitors
- Aerogel capacitors

This application note will conform to the classification and terms shown in Figure 1.

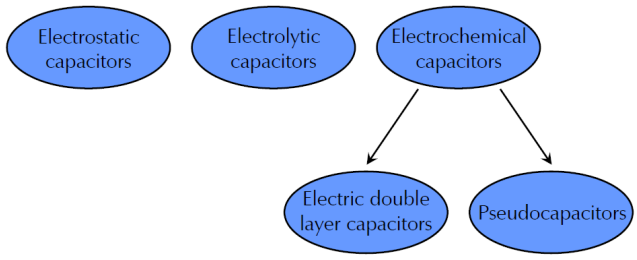

Figure 1 – Classification and designation of capacitors.

Figure 1 shows a schematic diagram of the classification of capacitors divided into three major groups:

Electrostatic capacitors use metal plates as electrodes that are separated by a dielectric with low conductivity, e.g. ceramics, glass, or even air.

Electrolytic capacitors use a metal foil as anode, e.g. aluminum or tantalum. During the anodizing process a metal oxide is formed which is used as dielectric. The cathode also consists of a metal foil.

Electrochemical capacitors use in contrast to electrostatic and electrolytic capacitors high-surface electrodes to increase capacitance. They can be divided in two subgroups depending on the storage mechanism.

- **Electric double layer capacitors** (EDLCs) use electrostatic charge separation to store energy. As the name says, a double layer is built up within the interface between electrolyte and electrode surface.
- **Pseudocapacitors** use beside electrostatic charge separation also highly reversible Faradaic surface reactions to store energy.

This application note uses only electrochemical capacitors for its measurements. Hence electrostatic and electrolytic capacitors will not be discussed.

Generally, EDLCs use activated carbon as electrode material. With surface areas of 1000 m^2/g or more capacitances of 200 F/g can be reached. Pseudocapacitors use among others transition metal oxides (e.g. RuO_2) or polymers as electrode materials.

To discuss several electrochemical techniques tests were performed on two different ECs in this note. Commercial 3 F EDLCs from Nesscap (P/N ESHSR-0003C0-002R7) and a 1 F PAS pseudocapacitor from Taiyo Yuden (P/N PAS0815LR2R3105) were used. The acronym PAS stands for Polyacenic Semiconductor which is a conductive polymer deposited on the electrodes.

The data in this note were recorded using Gamry's PWR800 software. All plots were generated and evaluated using Gamry's Echem Analyst.

Ideal Capacitor Characteristics

A capacitor is a storage device for electrical charge. A capacitor's state-of-charge is easily measured. The stored charge of an ideal capacitor is proportional to the voltage, given by Equation 1:

$$Q = C \cdot U \qquad \text{Eq 1}$$

Q is the capacitor's charge in ampere-seconds (As) or coulombs (C), C is the capacitance in farads (F), and U is the voltage between the device's terminals in volts (V).

The energy E stored in a capacitor can be calculated by Equation 2. The unit for the energy is joule (J):

$$E = \tfrac{1}{2} C \cdot U^2 \qquad \text{Eq 2}$$

An ideal capacitor with no current flow will store energy and charge for ever.

Power drawn from a capacitor during charge or discharge is proportional to the capacitor's voltage and the electrical current, given by Equation 3:

$$P = U \cdot I \qquad \text{Eq 3}$$

P is the power in watts (W) and I is the electrical current in amperes (A). An ideal capacitor loses no power or energy during charge or discharge.

Capacitor Non-ideality

The ideal capacitor does not exist. In reality, capacitors have always limitations and imperfections. The tests in this application note illustrate these limitations.

Voltage limitations

The description of ideal capacitors did not mention voltage limitations. Capacitors can only operate within a "voltage window" with both an upper and lower voltage limit. Voltages outside this window can cause electrolyte decomposition damaging the device.

The range of the voltage window strongly depends on the electrolyte which can be aqueous or non-aqueous. Generally, aqueous electrolytes are safer and easier to use. However, capacitors with non-aqueous electrolytes can have a much wider voltage window.

Commercial single-cell ECs currently have an upper voltage limit below 3.5 V. For high-voltage applications multiple cells in series are used.

All commercial ECs are specified to be unipolar – the voltage on the plus (+) terminal must be more positive than the voltage on the minus (-) terminal. The lower voltage limit is usually zero volts.

ESR

Real capacitors suffer from power loss during charge and discharge. This loss is caused by resistances in electrical contacts, electrodes, and electrolyte. The sum of these resistances is called *Equivalent Series Resistance* (ESR). For ideal capacitors ESR is zero. It is specified on the data sheet for most commercial capacitors.

The power loss P_{Loss} during charge or discharge is given by Equation 4:

$$P_{Loss} = I^2 \cdot ESR \qquad \text{Eq 4}$$

This power is lost as heat – under extreme conditions enough heat to damage the device.

The ESR can be modeled as a resistor in series with an ideal capacitor.

Leakage current

Ideal capacitors maintain constant voltage without current flow from an external circuit. Real capacitors require a current, called leakage current $I_{leakage}$, to maintain constant voltage.

Leakage current will slowly discharge a charged capacitor that has no external connections to its terminals. This process is called self-discharge.

$I_{leakage}$ can be calculated using Equation 5, multiplying the capacitance by the rate of voltage change:

$$I_{leakage} = C\frac{dU}{dt} \qquad \text{Eq 5}$$

Leakage current can be modeled as resistor that is parallel with a capacitor. This model is a simplification of the voltage and time dependence of leakage current.

As an example, a leakage current of 1 μA on a 1 F capacitor held at 2.5 V implies a 2.5 MΩ leakage resistance. The time constant for the self-discharge process would be $2.5 \cdot 10^6$ seconds – nearly a month.

Time effects

The time constant τ for a charge or discharge process of an ideal capacitor in series with an ESR can be calculated by Equation 6:

$$\tau = ESR \cdot C \qquad \text{Eq 6}$$

Typically, τ is between 0.1 and 20 seconds. A voltage step into a capacitor with ESR should create a current that exponentially decays towards zero. In a device with leakage current, the post-step current decay stops at the leakage current.

Time effects can be caused by slow Faradaic reactions occurring at imperfections on the surface of the electrode material. Carbon surfaces used for most electrochemical capacitors have oxygen containing groups (hydroxyl, carbonyl…) that are plausible reaction sites.

Commercial ECs do not show this simple behavior. As seen further below, commercial capacitors held at a constant potential take days to reach their specified leakage current. The time needed is much greater than predicted by τ.

Dielectric absorption is a phenomenon that can also occur on capacitors. It is a short-term time effect and is caused by non-electrostatic charge storage mechanisms with very long time constants.

Time effects also can be a side effect of porosity inherent in high-capacity electrodes. The farther inside a pore, the more increases the electrolyte resistance. Hence different areas of the electrode surface see different resistances.

As discussed more precisely in part 3 of this note, this complicates the simple capacitor model into a distributed element that is also called transmission line model.

Cycle-life

An ideal capacitor can be charged and discharged for an infinite number of cycles. Many commercially available ECs approach this ideal – they are specified for 10^5 or even 10^6 charge/discharge cycles.

In contrast, secondary batteries' cycle-life specifications are typically hundreds of cycles.

The cycle-life for all rechargeable devices depends on the exact conditions under which cycling occurs. Applied current, voltage limits, device history, and temperature are all important. Part 2 will go more into detail.

Cyclic Voltammetry

Cyclic Voltammetry (CV) is a widely used technique in electrochemistry. Early in a development project, CV yields basic information about a capacitive electrochemical cell, including:

- Voltage window
- Capacitance
- Cycle-life

A comprehensive description of CV is well beyond the scope of this document. Most books describing laboratory electrochemistry will have at least one chapter discussing CV.

Description of CV

In a cyclic voltammogram the current *I* that flows through an electrochemical cell is plotted versus the voltage *U* that is swept over a given voltage range.

A linear voltage ramp is used in the sweep. Often, a CV test will repetitively sweep the voltage between two limiting potentials. A pair of voltage sweeps in opposite directions is called a cycle.

A voltage sweep applied to an ideal capacitor creates a current given by Equation 7:

$$I = \frac{dQ}{dt} = C\frac{dU}{dt} \qquad \text{Eq 7}$$

dU/*dt* is the scan rate of the linear voltage ramp. For EC testing the rate is usually between 0.1 mV/s and 1 V/s.

Scan rates at the lower end of this range allow slow processes to occur but take a lot of testing time. Fast scan rates often show lower capacitances than slower scan rates. This effect will be discussed below.

Note that fast scans on high capacitance ECs may require more current than the instrument can output or measure. The maximum allowed scan rate can be calculated by rearranging Equation 7 and using the instrument's maximum current.

Figure 2 shows a typical CV experiment. The capacitor voltage and current are plotted versus time. The darker colored, saw-toothed waveforms are the voltage applied to the cell, the lighter colored curves are the current. Three and a half cycles are shown, each in a different color.

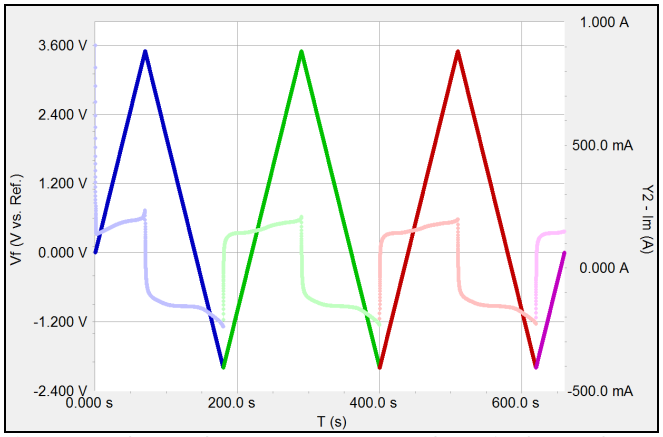

Figure 2 – Voltage and current versus time are shown for three and a half cycles. For details, see text.

Figure 3 shows Gamry's PWR800 setup for a CV test. Four voltage parameters define the sweep range. The scan starts at ***Initial E***, ramps to ***Scan Limit 1***, reverses, and goes to ***Scan Limit 2***. Additional cycles start and end at Scan Limit 2. The scan ends at the ***Final E***.

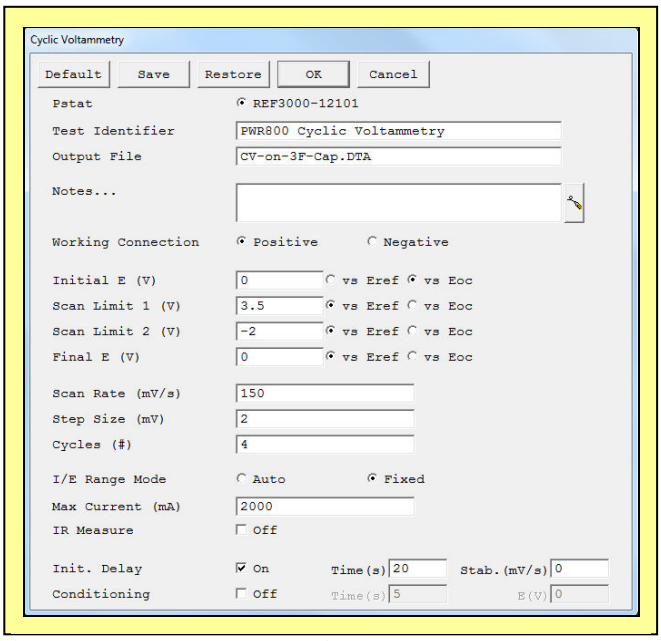

Figure 3 – Gamry's PWR800 setup for a CV experiment.

CV experiments can be run with two-electrode or three-electrode cell connections.

Three-electrode configurations are common in fundamental research where it allows one electrode to be studied in isolation, without complications from the electrochemistry of the other electrodes. The three electrodes are:

- Working Electrode – the electrode being tested.
- Reference Electrode – an electrode with a constant electrochemical potential.
- Counter Electrode – generally an inert electrode, present in the cell to complete the electric circuit.

Testing of packaged capacitor requires two-electrode connections. All potentiostats can operate with this cell configuration.

The setup for a two-electrode cell configuration with a Gamry Instruments system is easy. Both Reference (white) and Counter electrode leads (red and orange) are connected to the minus (-) terminal of the capacitor. Working electrode (green) and Working sense lead (blue) are connected to the opposite plus (+) terminal.

Theoretical CV plot

Figure 4 shows a theoretical CV plot for a 3 F EDLC in series with a 50 mΩ ESR. The scan rate is 100 mV/s. The scan limits were:

- Initial E: 0.0 V
- Final E: 0.0 V
- Scan Limit 1: +2.4 V
- Scan Limit 2: -0.5 V

The scan's start is shown on the plot along with arrows showing the direction of the scan. The second cycle is shown in red.

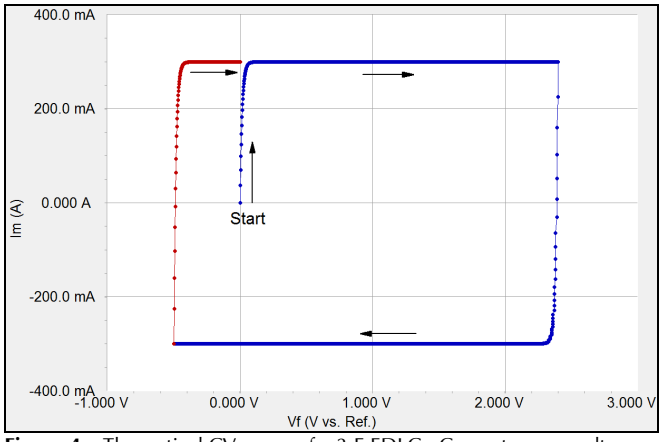

Figure 4 – Theoretical CV curve of a 3 F EDLC. Current versus voltage are shown for the first two cycles. For details, see text.

For an ideal capacitor (with no ESR) the shape of the CV diagram would be a rectangle. The height for a charge and discharge step can be calculated using Equation 7:

$$I = C\frac{dU}{dt} = 3\,\mathrm{F}\cdot 100\,\mathrm{mV/s} = 300\,\mathrm{mA}$$

In reality, ESR causes slow rise in the current and rounds two corners of the rectangle at the beginning of the charge and discharge process. The time constant τ affects the rounding of the corners.

CV on a 3 F EDLC

Figure 5 shows a cyclic voltammogram of a 3 F EDLC. This experiment illustrates how CV plots can be used to determine a capacitor's voltage window.

The scan rate was 100 mV/s. The voltage limits for the experiment were initially set to +5 V and -3 V which is well beyond the 2.7 V specification of the EDLC.

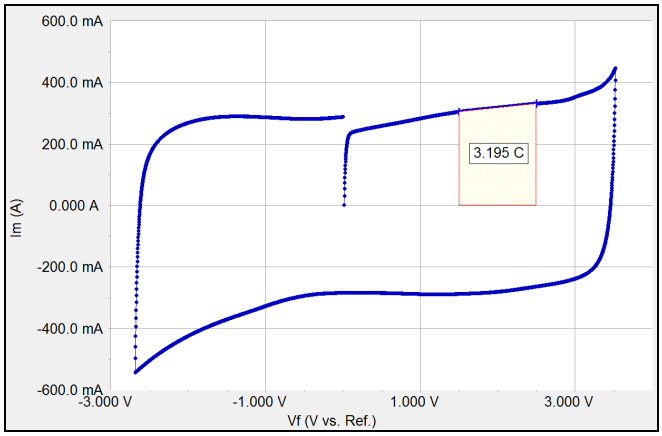

Figure 5 – CV curve of a 3 F EDLC. Current versus voltage are shown for the first cycle. For details, see text.

Notice this plot's differences in current behavior to the theoretical CV plot shown in Figure 4. The CV curve does not look like a rectangle.

The scan was manually reversed when the current started to increase dramatically. Selecting **F2-Skip** in Gamry's Framework reverses a sweep.

The first reversal occurred at +3.5 V. Increasing current indicated the beginning of electrolyte decomposition. At the back scan current did start to increase below 0 V. The sweep was manually reversed at -2.7 V.

By integration of a segment of this curve the stored charge can be calculated. The charge is automatically calculated by the software. The integrated area is highlighted red in Figure 5.

The integration range was selected using the Echem Analyst's ***Select Range Using Keyboard*** function.

The calculated charge between 1.5 V and 2.5 V is 3.195 C. Using Equation 1, the capacitance of the device can be calculated:

$$C = \frac{Q}{U} = \frac{3.195\,\mathrm{C}}{2.5\,\mathrm{V} - 1.5\,\mathrm{V}} = 3.195\,\mathrm{F}$$

The calculated capacitance depends on the CV scan rate, the voltage region, and a variety of other variables.

Important Note: Capacitor non-ideality precludes calculation of a true capacitance value for a real EC. Commercial ECs have a specified capacitance that is only valid when a specific experiment is used. Note, techniques such as CV, long-term potentiostatic and galvanostatic tests, and EIS can give very different capacitance values.

CV normalized by scan rate

Figure 6 shows CV curves of a second 3 F EDLC used to explain the scan rate dependence on CVs.

Scan rates of 3.16, 10, 31.6, 100, and 316 mV/s were used. The capacitor was held at 0 V for 10 minutes between the scans. The scan limits were set to 0 V and 2.7 V.

Gamry's ***Sequence Wizard*** is a convenient tool for setting up complex experiments like this. The 0 V delay and the CV test were put inside a loop. The scan rate was multiplied by √10 after each cycle.

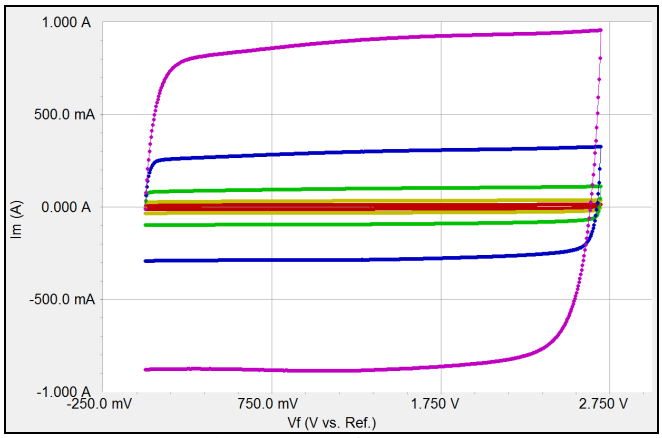

Figure 6 – CV curves of a 3 F EDLC with varying scan rates. (●) 316 mV/s, (●) 100 mV/s, (●) 31.6 mV/s, (●) 10 mV/s, (●) 3.16 mV/s. For details, see text.

All CV curves show the same shape. ESR leads to rounded corners in the CV curve. Differences occur in the current that increases with increasing scan rate.

Figure 7 shows the same CV curves normalized by dividing all currents by the scan rate.

After normalization, the Y-axis unit is As/V which corresponds to capacitance in farads. This note will call the Y-axis of a normalized CV plot apparent capacitance C_{app}.

Use in the Echem Analyst's CV menu the ***Normalize By Scan Rate*** command to normalize CV data. Select each single curve using the Curve Selector before executing this command. Normalization creates a new curve with *NSR* in its filename.

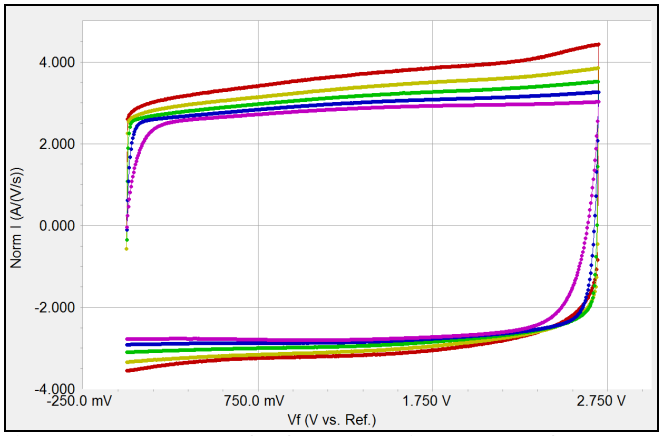

Figure 7 – Scan rate normalized CV curves of a 3 F EDLC with varying scan rates. (●) 316 mV/s, (●) 100 mV/s, (●) 31.6 mV/s, (●) 10 mV/s, (●) 3.16 mV/s. For details, see text.

For ideal capacitors, scan rate normalized CV curves superimpose and capacitance does not depend on the scan rate.

However, EDLCs are not ideal and scan rate normalized curves do not superimpose. In Figure 7, C_{app} is around 2.5 F on the curve with the highest scan rate. This curve resembles the CV curve of an ideal capacitor plus ESR.

As scan rate decreases, C_{app} rises and shows stronger voltage dependence. This phenomenon is expected for voltage-driven chemical reactions.

The increase in C_{app} by decreasing scan rate can be explained by kinetically slow Faradaic reactions on the electrode surface and by transmission line behavior caused by electrode porosity.

In the case where slow surface reactions are present, fast scans are over before reactions occur – all current is due to capacitance. Faradaic current has time to flow when scan rates are slower, increasing total current and C_{app}.

A distributed element model will show a similar scan rate behavior. An electrode surface with a high electrolyte resistance will not have time to respond to voltage changes during a fast scan. In effect, the fraction of electrode surface accessible to the electrolyte depends on the scan rate.

CV used to estimate cycle-life

Cyclic voltammetry can also differentiate between poor cycle-life and potentially useful cycle-life.

Figure 8 shows the result of a CV experiment with a 3 F EDLC. 50 cycles between 1.5 V and 2.7 V were recorded. The 1st, 10th, and 50th cycles are shown. The scan rate for this test was 100 mV/s.

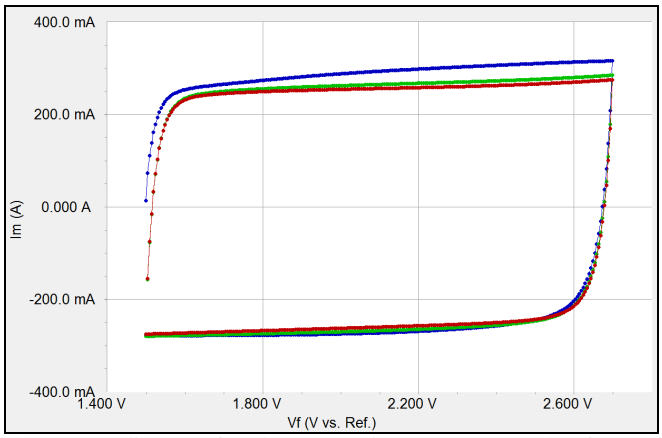

Figure 8 – Different cycles of a CV test of a 3 F EDLC. (●) 1st cycle, (●) 10th cycle, (●) 50th cycle. For details, see text.

The first cycle exhibits a quite bigger current compared to the others. Initial electrochemical reactions that occur on the surface of the electrodes lead to higher currents. After a while the EC is in steady-state and differences in cyclic voltammograms are minor.

There is very little change in the data between the 10th and the 50th cycle. Hence this capacitor could be worth of cycle-life testing using cyclic charge-discharge techniques, described in part 2 of this application note.

CV on a pseudocapacitor

CV measurements on pseudocapacitors differ from the results measured on an EDLC.

Figure 9 shows a CV test on a 1 F PAS pseudocapacitor. Scan rate was set to 3.16, 10, 31.6, 100, and 316 mV/s. The scan range varied from 0 V to 2.4 V. The capacitor rested at 0 V for 10 minutes between the scans. The curves are normalized by scan rate.

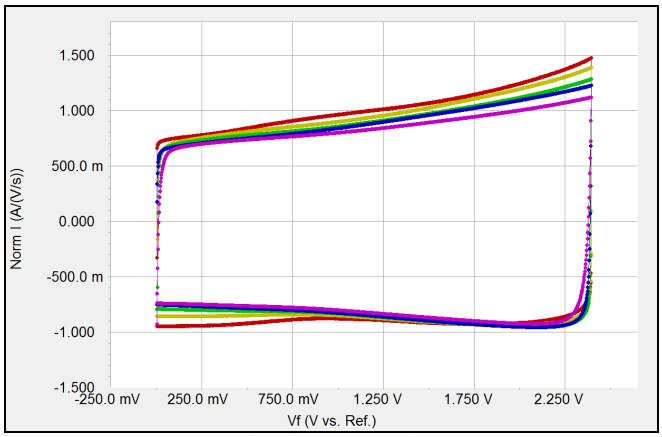

Figure 9 – Scan rate normalized CV curves of a 1 F PAS pseudocapacitor with varying scan rates. (●) 316 mV/s, (●) 100 mV/s, (●) 31.6 mV/s, (●) 10 mV/s, (●) 3.16 mV/s. For details, see text.

There is one major difference compared to normalized CV plots of EDLCs (Figure 7). At higher scan rates the CV

plots do not superimpose. The device's C_{app} depends on voltage at all scan rates. This is expected, given the Faradaic nature of charge storage of pseudocapacitors.

Leakage Current Measurement

Leakage current can be measured in at least two ways:

- Apply a DC voltage to a capacitor and measure the current required to maintain that voltage.
- Charge a capacitor to a fixed voltage. Then measure the change of the open circuit potential of the capacitor during self-discharge.

Conway's book includes a chapter discussing leakage current and self-discharge of electrochemical capacitors.

In an attempt to make the specifications of an EC look good, some manufacturers specify leakage current that is measured after 72 hours. Under these conditions, leakage current can be as low as 1 μA/F.

Direct leakage current measurement

Direct potentiostatic measurement of leakage current is quite challenging. A DC potential must be applied to the capacitor and very small currents must be measured.

Typically, charging currents are in amps and leakage currents are in microamps, a range of 10^6. Noise and/or drift in the DC potential can create currents that are larger than the leakage current itself.

For example, assume the 3 F EDLCs used in this note have an ESR of 100 mΩ. To measure leakage currents of 1 μA on these capacitors current noise should be less than the 1 μA signal.

At frequencies where ESR dominates the impedance, 0.1 μV of noise in the applied voltage will create a noise in current of 1 μA. At lower frequencies, where capacitance dominates the impedance, a voltage drift of 0.3 μV/s creates a current of 1 μA.

Fast data acquisition, external noise sources, or lack of a Faraday cage can lead to large apparent DC currents or continual switching between current ranges.

A special script has been developed for direct leakage current measurement using the PWR800 software. This script was added to Gamry's Framework in Rev. 5.61 and is named:

PWR Leakage Current.exp

The special script uses a user entered estimate for ESR to avoid I/E converter ranges where voltage noise can overload the current measurement circuitry. Do not use the potentiostatic test in Gamry's PWR800 software to measure leakage currents.

Figure 10 shows a leakage current measurement on a new 3 F EDLC. $I_{leakage}$ is plotted logarithmically versus time and was measured for five days. The capacitor was charged to 2.5 V potentiostatically and held at this potential.

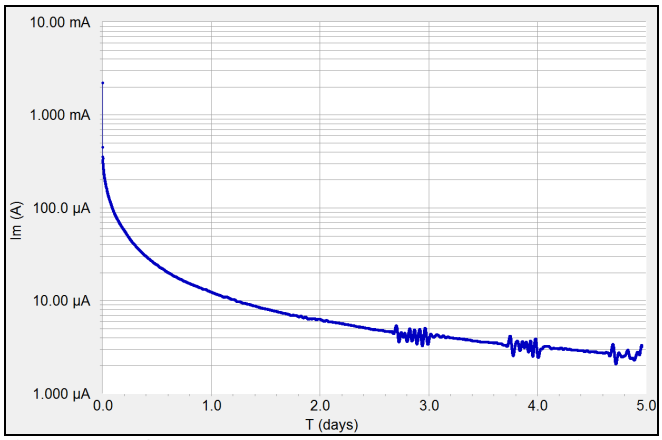

Figure 10 – Leakage current measurement on a 3 F EDLC over five days at 2.5 V. For details, see text.

$I_{leakage}$ is still falling five days after applying the potential. After 72 hours the measured current was about 4.2 μA, after five days it reached 3.2 μA. The manufacturer specifies leakage current on this capacitor at less than 5 μA after 72 hours.

Note the periodic noise signal at low currents that is caused by daytime air conditioning. The data in this plot was smoothed using a Savitzky-Golay algorithm with a 60 second window.

Measurement of self-discharge

Self-discharge causes the open-circuit voltage of a charged capacitor to decrease over time. Leakage current discharges the capacitor during self-discharge – even though there is no external electrical current.

Conway's book describes three different mechanisms for self-discharge. They can be distinguished by analyzing the shapes in voltage versus time curves recorded over long time periods. This analysis was not done on the data presented here.

Figure 11 shows the diagram of a self-discharge measurement. A 3 F EDLC was first charged to 2.5 V and the potential was held for 12 hours. The open-circuit voltage was measured and recorded versus time.

The self-discharge measurement was done with a special script. This script was added to Gamry's Framework in Rev. 5.61 and is named:

PWR Self-Discharge.exp

Use in the Echem Analyst's Common Tools menu the *Linear Fit* function to calculate the slope of the curve.

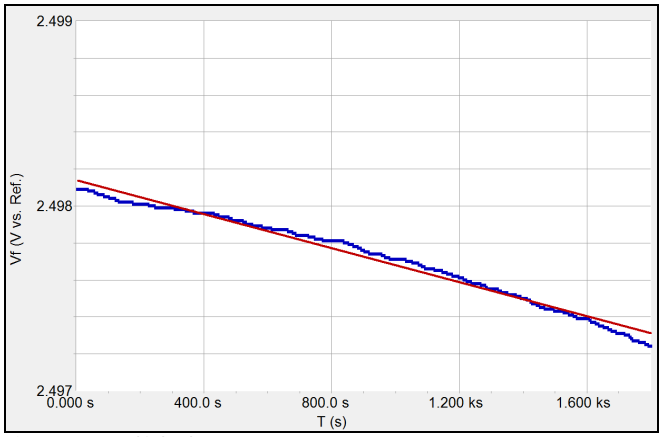

Figure 11 – Self-discharge measurement on a 3 F EDLC.
(●) Linear-least-square fit. For details, see text.

Voltage change for this capacitor was less than 2 mV after 30 minutes. The red line is a linear-least-square fit of the voltage decay data. The slope of the line is 0.55 μV/s. The leakage current can be calculated using Equation 5:

$$I_{leakage} = 3\,\mathrm{F} \cdot 0.55\,\mu\mathrm{V/s} = 1.65\,\mu\mathrm{A}$$

Conclusion

This application note discussed theoretical and practical basics of electrochemical capacitors.

Fundamental mathematical equations were explained and the right classification of capacitors was shown.

Gamry's PWR800 cyclic voltammetry test setup was introduced. Based on this, CV measurements were performed on EDLCs and pseudocapacitor to show differences of these energy storage devices.

Further on, two different methods were shown to measure leakage current. For this, Gamry Instruments offers two special scripts.

Testing Electrochemical Capacitors, Part 1 – Cyclic Voltammetry and Leakage Current. Rev 1.02 3/14/2012

734 Louis Drive • Warminster, PA 18974, USA • Tel. 215 682-9330 • Fax 215 682-9331 • www.gamry.com • info@gamry.com