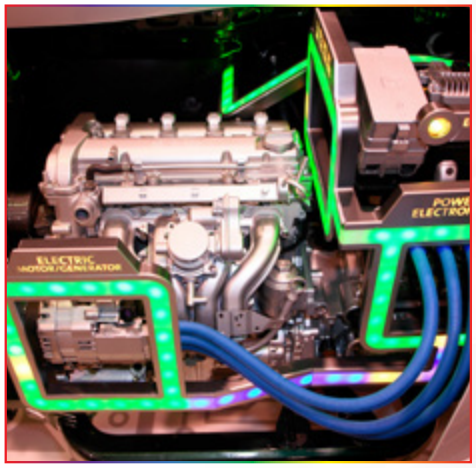
White Paper

Testing Super-Capacitors



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Part 1: CV, EIS, and Leakage Current

Introduction

Super-capacitors are energy storage devices similar to secondary batteries. Unlike batteries, which use chemical reactions to store energy, super-capacitors generally store energy through the physical separation of electrical charges.

All super-capacitors consist of two electrodes immersed in a conductive liquid or conductive polymer called the electrolyte. The electrodes are separated by an ionic-conducting separator that prevents shorts.

Compared to a battery, a super-capacitor has the following advantages.

- Higher charge and discharge rates (high power density)
- Longer cycle life (>100,000 cycles)
- Materials with low toxicity
- Operation over a wide temperature range
- Low cost per cycle

These are offset by some disadvantages:

- Higher self-discharge rate
- Lower energy density
- Lower cell voltage
- Poor voltage-regulation
- High initial cost

Current applications for super-capacitors include:

- Hybrid electric vehicles (HEVs)
- Diesel-engine starting systems
- Cordless power tools
- Emergency and safety systems

Many applications use a super-capacitor in parallel with a battery, a combination with a better cycle-life and higher power than the battery alone. For more information read Brian Conway's book on super-capacitor technology.[1]

This application note is the first part of a two-part overview of the electrochemical techniques used to test a super-capacitor device or technology. Part 1 discusses techniques familiar to electrochemists, while Part 2 discusses techniques familiar to battery technologists. Part 3 discusses the basics of electrochemical impedance spectroscopy (EIS) as well as Gamry's EIS techniques.

Commercial capacitors were tested to obtain results used in discussion of techniques. The data were acquired using a Gamry Instruments Reference 3000 Auxiliary Electrometer. All plots were generated using Gamry's Echem Analyst software.

Items in yellow boxes are specific to Gamry products.

Similar Technology, Confusing Names

A traditional Electrical Double-Layer Capacitor (EDLC) uses electrostatic charge storage to store energy. Electrons in each electrode and ions in the electrolyte form a double-layer capacitor. Typical capacitance of an electrochemical double layer is 20 μF/cm^2. Capacitance of micro-porous carbon with a surface area of 1000 m^2/g can be as high as 200 F/g.

Some devices, which we call pseudo-capacitors, store charge via reversible Faradaic reactions on the surface of one or both electrodes. When electrode voltage is proportional to surface coverage and surface coverage is proportional to state-of-charge, these devices behave identically to capacitors. See Conway's book[1] for details concerning these devices.

Unfortunately, technical papers and commercially available products have used many names for EDLCs and pseudo-capacitors. These include:

- Super-capacitors
- Ultra-capacitors
- Aerogel capacitors
- Electrical double-layer capacitors

Unless otherwise noted, this note uses the term super-capacitor for all high-capacitance devices, regardless of charge-storage mechanism.

1. B.E. Conway, Electrochemical Supercapacitors: Scientific Fundamentals and Technological Applications, New York: Kluwer Academic Press/Plenum Publishers, 1999.

Ideal Capacitors

A capacitor is a storage device for an electrical charge. The voltage of an ideal capacitor is proportional to the charge stored in the capacitor:

$CV = Q$ Eq.1

C is capacitance in farads;

V is voltage between the device's terminals in volts;

Q is the capacitor's charge in Coulombs, in ampère-seconds.

A capacitor's state-of-charge is easily measured: it is proportion to voltage. In contrast, measuring a battery's state of-charge can be difficult.

The energy stored in a capacitor is:

$E = \frac{1}{2}CV^2$ Eq.2

E is the energy in joules.

The power drawn from a capacitor during discharge depends on the capacitor's voltage and the electrical current:

$P = VI$ Eq.3

P is power in watts;

V is the capacitor voltage in volts;

I is the discharge electrical current in ampères.

An ideal capacitor loses no power or energy during charge or discharge, so the equation above can also be used to describe the charge process. An ideal capacitor with no current flow will store energy and charge forever.

Non-ideal Capacitors

The ideal capacitor does not exist, for real capacitors have limitations and imperfections. The tests in this white paper measure these limitations.

Voltage Limitations

The description of ideal capacitors did not mention voltage limitations. Capacitors can only operate within a "voltage window" with both an upper and lower voltage limit. Voltages outside the window can cause electrolyte decomposition damaging the device.

Capacitor electrolytes may be aqueous or non-aqueous. While aqueous electrolytes are generally safer and easier to use, capacitors with non-aqueous electrolytes can have a much wider voltage window.

When this was written, commercial single-cell super-capacitors had an upper voltage limit below 3.5 V. High-voltage devices have multiple cells in series.

All commercial super-capacitors are specified to be unipolar: the voltage on the plus (+) terminal must be more positive than the voltage on the minus (–) terminal. The lower voltage limit is therefore zero.

ESR

Real capacitors suffer power-loss during charge and discharge. The loss is caused by resistance in the electrodes, contacts, and in the electrolyte. The standard term for this resistance is Equivalent Series Resistance (ESR). ESR is specified on the data sheet for most commercial capacitors.

One of the simplest models for a real capacitor is ESR in series with an ideal capacitor. The power loss, P_{loss}, during charge or discharge is ESR times the current squared:

$$P_{loss} = I^2 \cdot ESR \qquad \text{Eq.4}$$

This power is lost as heat—under extreme conditions enough heat to damage the device.

Leakage Current

Leakage current is another capacitor non-ideality. An ideal capacitor maintains constant voltage without current flow from an external circuit. Real capacitors require current, called leakage current, to maintain a constant voltage.

Leakage current can be modeled as a resistance in parallel with the capacitor. This model oversimplifies the voltage-and time-dependence of leakage current.

Leakage current discharges a charged capacitor that has no external connections to its terminals. This process is called self-discharge.

Note that a leakage current of 1 μA on a 1 F capacitor held at 2.5 V implies a 2.5 MΩ leakage resistance. The time constant for the self-discharge process on this capacitor is 2.5×10^6 seconds—nearly a month.

Time Effects

The time constant, τ, for charge or discharge of an ideal capacitor in series with ESR is:

$$\tau = ESR \cdot C \quad \text{Eq.5}$$

Typically τ is between 0.1 and 20 seconds. A voltage step into a capacitor with ESR should create a current that exponentially decays toward zero. In a device with leakage current, the post-step current-decay stops at the leakage current.

Commercial super-capacitors do not show this simple behavior. As seen below, commercial capacitors held at constant potential often take days to reach their specified leakage current. The time needed is much greater than predicted by τ.

One short-term time effect on a capacitor is a phenomenon electrical engineers call dielectric absorption. Dielectric absorption is caused by non-electrostatic charge-storage mechanisms with very long time constants.

Time effects may be caused by slow Faradaic reactions occurring at imperfections on the surface of the electrode material. The carbon surfaces used for most super-capacitors have oxygen-containing groups (hydroxyl, carbonyl, and so on) that are plausible reaction sites.

Time effects might also be a side effect of the porosity inherent in high-capacity electrodes. Electrolyte resistance increases with distance into a pore. Different areas of the electrode surface therefore see different resistances. As discussed below, this complicates the simple-capacitor-plus-ESR model into a distributed-element or transmission-line model.

Cycle life

An ideal capacitor can be charged and discharged for an infinite number of cycles. Many commercial super-capacitors approach this idea: they are specified for 10^5 or even 10^6 charge/discharge cycles. Secondary battery cycle life specifications are typically hundreds of cycles.

The cycle life for all rechargeable devices depends on the exact conditions under which cycling occurs. Currents, voltage limits, device history, and temperature are all important.

Cyclic Voltammetry (CV)

Cyclic Voltammetry (CV) is a widely-used electrochemical technique. Early in a capacitor development project, CV yields basic information about a capacitive electrochemical cell including:

- Voltage window
- Capacitance
- Cycle life

A comprehensive description of CV is well beyond the scope of this application note. Most books describing laboratory electrochemistry have at least one chapter discussing CV.

Description of CV

CV plots the current that flows through an electrochemical cell as the voltage is swept over a voltage range. A linear voltage-ramp is used in the sweep. Often, a CV test repetitively sweeps the voltage between two limit potentials. A pair of sweeps in opposite directions is called a cycle.

Figure 1 presents a CV experiment as a plot of capacitor voltage and current versus time. The darker-colored, saw-toothed waveforms are the voltage applied to the cell; the lighter-colored waveforms are measured current. This graph shows a CV test with three and one-half cycles. Each cycle is shown in a different color.

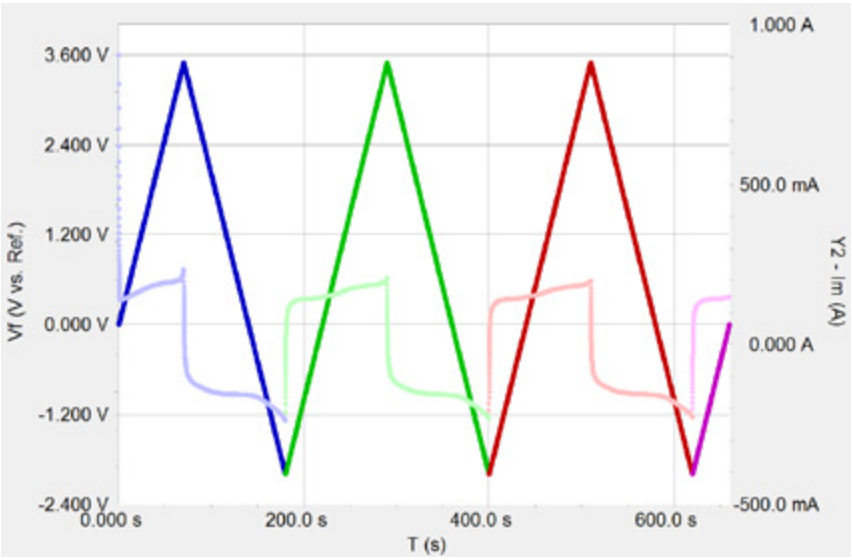


Figure 1. Cyclic Voltammetry as capacitor voltage vs. time. Darker lines are applied voltage; lighter lines are the measured current. Each cycle is a different basic color.

CV may be run with two-electrode or three-electrode cell connections.

Three-electrode connections are common in fundamental research, to allow one electrode to be studied in isolation—without complications from the electrochemistry of the other electrodes. The three electrodes are:

- Working electrode, the electrode being tested.
- Reference electrode, an electrode with a constant electrochemical potential.
- Counter electrode, generally an inert electrode present in the cell to complete the circuit.

Figure 2 shows Gamry's setup for a CV test.

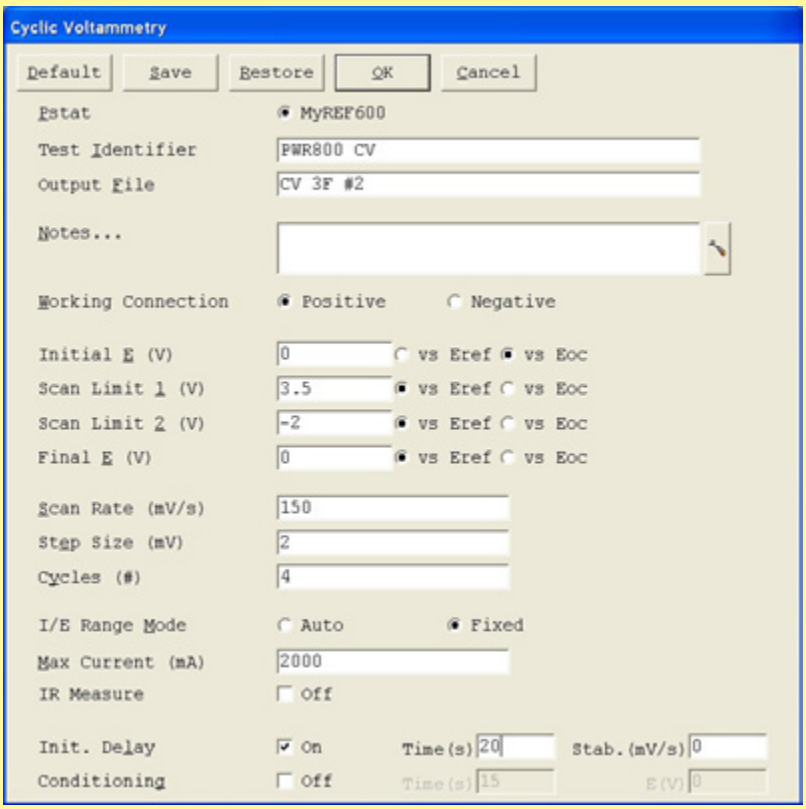


Figure 2. Cyclic Voltammetry set-up window. *Four voltage parameters define Gamry's CV sweep range. The scan starts at the* ***Initial E****, ramps to Scan Limit 1, reverses and goes to* ***Scan Limit 2****. Additional cycles start and end at Scan Limit 2. The scan ends at the* ***Final E****.*

Testing packaged capacitors requires two-electrode connections. All potentiostats can operate with two-electrode connections. Simply connect both the reference electrode and the counter electrode leads to one side of the capacitor. Connect the working electrode lead (and working sense lead, if present) to the other side.

A voltage sweep applied to an ideal capacitor creates a current given by

$$I = \frac{dQ}{dt} = C\frac{dV}{dt} \quad \text{Eq.6}$$

where I is current in amperes, and $\frac{dV}{dt}$ is the scan rate of the voltage ramp.

Voltage scan rates for super-capacitor testing are usually between 0.1 mV/s and 1 V/s. Scan rates at the lower end of this range allow slow processes to occur, but take a lot of testing time. Fast scans often show lower capacitance than slower scans. This effect is discussed below.

Be careful: fast scans on high-value capacitors may require more current than the instrument can put out or measure. The maximum allowed scan rate is:

$$\left(\frac{dV}{dT}\right)_{max} = \frac{I_{max}}{C} \quad \text{Eq.7}$$

where I_{max} is the instrument's maximum current in amperes.

Theoretical CV Plot

CV is plotted with current on the y-axis and voltage on the x-axis. Figure 3 is a theoretical CV plot for a 3 F capacitor in series with a 50 mΩ ESR.

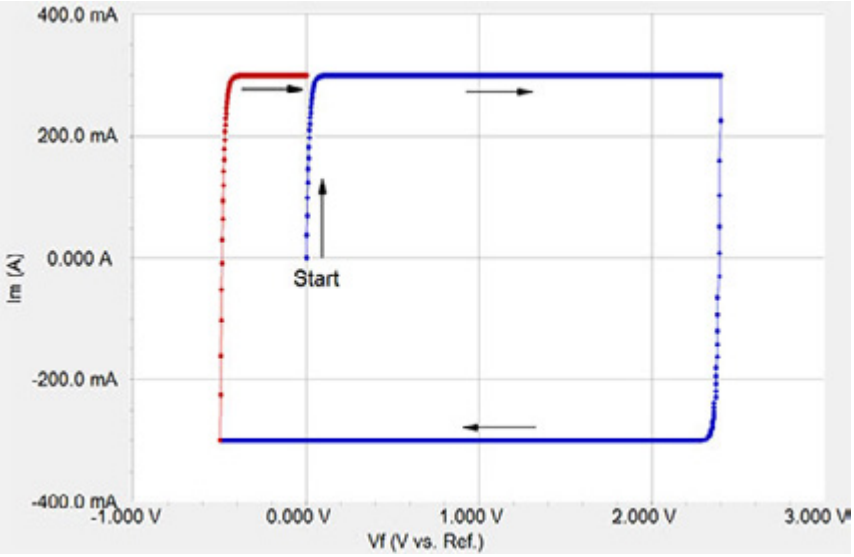


Figure 3. Theoretical cyclic voltammetry for 3 F capacitor in series with a 50 mΩ ESR.

The scan rate is 100 mV/s. The scan limits were:

- Initial E 0.0 V
- Scan Limit 1 2.4 V
- Final E 0.0 V
- Scan Limit 2 –0.5 V

The scan's Start is shown on the plot along with arrows showing the direction of the scan. The second cycle is shown in red.

If this CV were recorded on an ideal capacitor (with no ESR), the CV plot would be a rectangle, with height:

$$I = C\frac{dV}{dt} = 300\ \text{mA} \quad \text{Eq.8}$$

ESR causes the slow rise in the current at the scan's start and rounds two corners of the rectangle. The time constant *τ*, discussed above, controls rounding of corners.

CV on a 3 F EDLC Capacitor

Most of this note's data were recorded using commercial 3 F EDLC capacitors. The parts tested were Nesscap[2] part #ESHSR-0003C0-002R7.

The 100 mV/s cyclic voltammogram of a 3 F capacitor (Figure 4) illustrates how CV can determine a capacitor's voltage window. Notice this plot's similarity to the theoretical CV plot shown above.

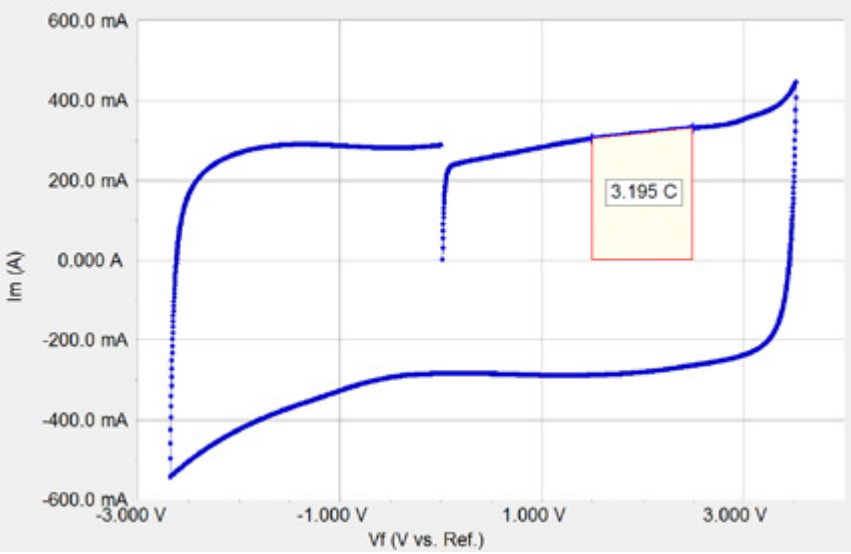


Figure 4. Cyclic voltammogram of 3 F capacitor between +5 V and –3 V, at 100 mV/s. Pink-shaded area is integration of one segment (1.5–2.5 V) of this curve.

The voltage limits entered in setup were +5 and –3 V. The scan was manually reversed when the current started to increase dramatically. The scan rate was slow enough that a user has time to react to the increased current. The reversal occurred at 3.5 volts, well beyond the 2.7 V specification for this capacitor. The negative going sweep was also manually reversed.

2. Nesscap Energy Inc., 24040 Camino Del Avion #A118, Monarch Beach, CA 92629, USA.

In Gamry's Framework software, selecting F2-Skip reverses a sweep.

Integrating a segment of this curve shows calculation of capacitance from CV data. The integrated region (between 1.5 and 2.5 V) is highlighted in pink shading.

Select the integration range using the Echem Analyst's ***Select Range Using Keyboard*** function.

Integration yielded the charge value shown on the curve. Capacitance is calculated from Q and the voltage range that was integrated:

$$C = \frac{Q}{\Delta V} = \frac{3.195\ \text{C}}{1\ \text{V}} = 3.195\ \text{F} \quad \text{Eq.9}$$

The calculated capacitance depends on the CV scan rate, the voltage region used in the integration, and a myriad of other variables.

Capacitor non-ideality precludes calculation of a true capacitance value for a real-world super-capacitor. Commercial super-capacitors have a specified capacitance value, valid when measured using a specific experiment. Other experimental techniques, including CV, EIS, and many long-term potentiostatic and galvanostatic tests, can give very different capacitance values.

CV Normalized by Scan Rate

A second capacitor was used to show CV's scan-rate dependence. Voltammograms were recorded at scan rates of 3.16, 10, 31.6, 100, and 316 mV/s. The capacitor was held at 0.0 V for 10 min between scans. Scan limits were 0.0 and 2.7 V.

Gamry's ***Sequence Wizard*** is a convenient tool for setting up complex experiments like this. The zero-volt delay and a CV test were put inside a loop. The scan rate was multiplied by √10 between tests.

A plot of the data obtained from these scans is shown in Figure 5. The purple curve was recorded at the highest scan rate and the red curve at the lowest scan rate.

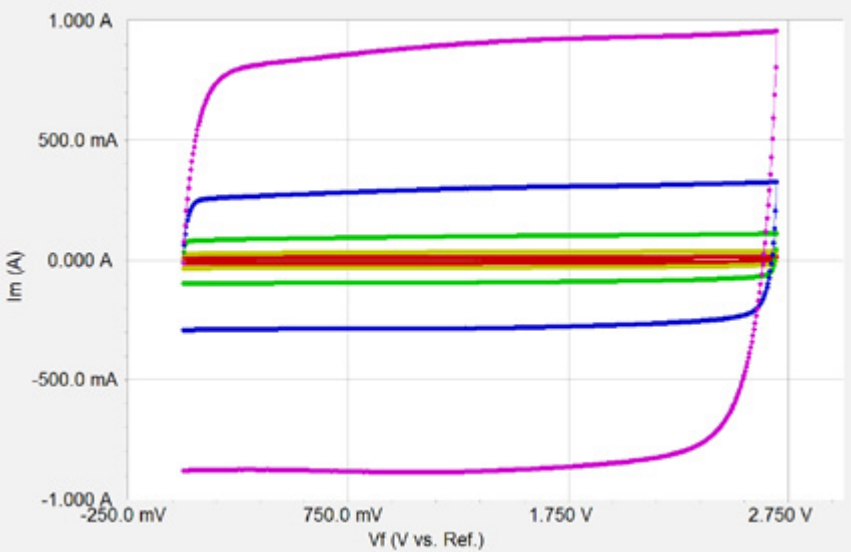


Figure 5. Dependence of cyclic-voltammetry data on scan rate. Purple is fastest; red is slowest.

Figure 6 shows these voltammograms normalized by dividing all currents by the scan rate.

Use the Echem Analyst's CV, ***Normalize By Scan Rate*** to normalize CV data. Select each curve in overlaid data using the ***Curve Selector*** before executing this command. Normalization creates a new curve with NSR in the curve's filename.

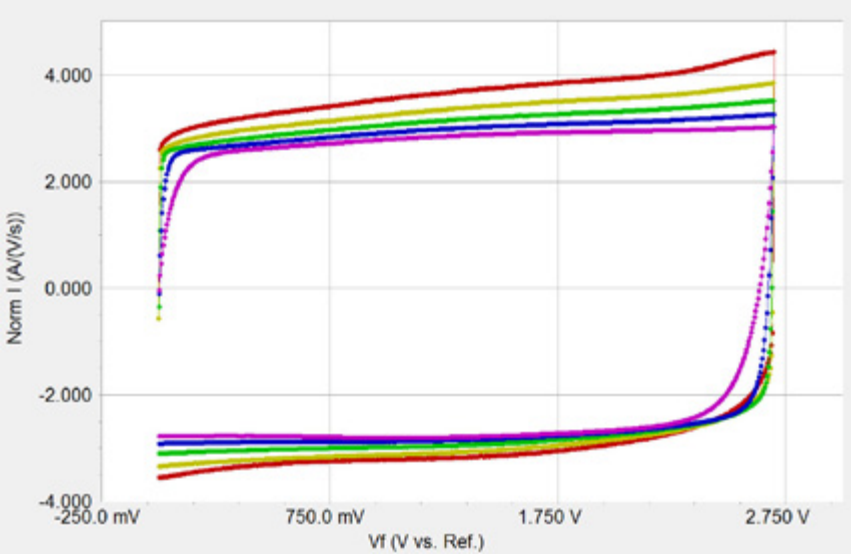


Figure 6. Same CV-data as Figure 4, but normalized to scan rate.

Scan-rate-normalized CV curves of an ideal capacitor superimpose: capacitance does not depend on scan rate. After normalization, the y-axis units of A·s·volt^{-1} become capacitance in farads.

Super-capacitors are not ideal, so normalized plots do not superimpose. This note calls the y-axis of a scan rate normalized CV apparent capacitance, C_{app}.

In Figure 6, C_{app} is ~2.5 F on the curve with the highest scan rate (purple). This curve resembles the CV of an ideal capacitor plus ESR. As scan rate decreases (blue, green, yellow, and red), the C_{app} rises and shows voltage dependence. This is expected for voltage-driven chemical reactions.

C_{app}'s scan-rate dependence can be explained by kinetically slow Faradaic reactions on the electrode surface and by transmission-line behavior caused by electrode porosity. Both cause an increase in C_{app} at lower scan rates.

In the case where slow surface reactions are present, fast scans are over before the reactions occur, so all current is caused by capacitance. Faradaic current has time to flow when scan rates are slower, increasing the total current and C_{app}.

A distributed-element model shows similar scan-rate behavior. Electrode surface that has high electrolyte resistance has no time to respond to voltage changes during a fast scan. In effect, the fraction of electrode surface accessible to the electrolyte depends on the scan rate.

CV to Estimate Cycle Life

CV can also differentiate between poor cycle life and potentially useful cycle life.

Figure 7, the CV plot below, shows 50 cycles between 1.0 and 2.7 V, recorded using a 3 F capacitor. The first, tenth, and fiftieth cycles are shown in blue, green and red.

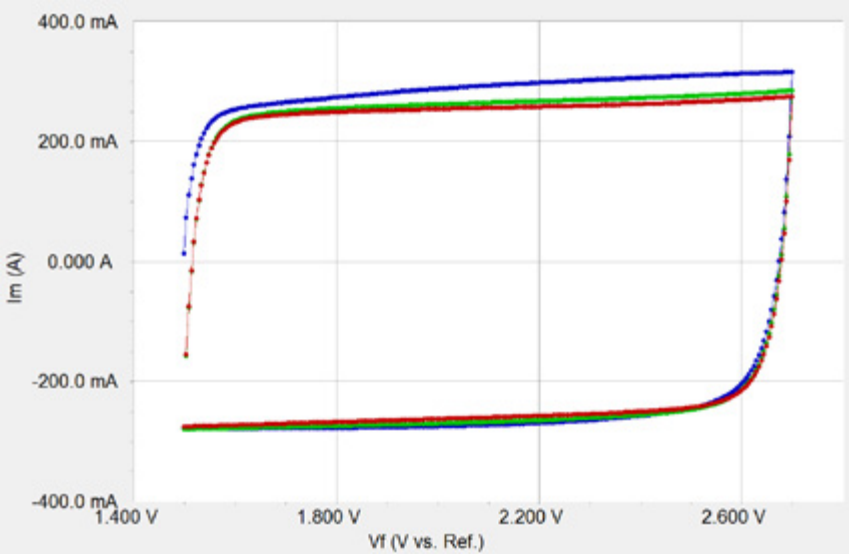


Figure 7. 50 cycles of CV data. (●) = cycle 1; (●) = cycle 10, and (●) = cycle 50.

There is very little change in the data between the tenth and the fiftieth cycles. Therefore, this capacitor is worthy of cycle-life testing using cyclic charge-discharge techniques (described in Part 2 of this application note).

CV on a Pseudo-capacitor

CV measurements on a pseudo-capacitor differ from the results measured on a true EDLC. We tested a 1 F PAS capacitor from Taiyo Yuden[3] (part number PAS0815LR2R3105). PAS stands for Polyacenic Semiconductor, which is a conductive polymer deposited on the electrodes.

CV tests were run on this device at 3.16, 10, 31.6, 100, and 316 mV/s. The scan range was 0.0 to 2.4 V. The capacitor rested at 0.0 V for 10 min between the scans.

Figure 8 shows the CV curves after normalization by scan rate. The red curve was recorded with the slowest scan rate and purple with the fastest. The y-axis is apparent capacitance.

When compared to the normalized CV plot for the EDLC in Figure 6, there is one major difference. The device's C_{app} depends on voltage at all scan rates. This is expected, given the Faradaic nature of charge storage in this pseudo-capacitor.

3. Taiyo Yuden (U.S.A.) Inc., 10 North Martingale Road, Suite 575, Schaumburg, Illinois 60173, USA.

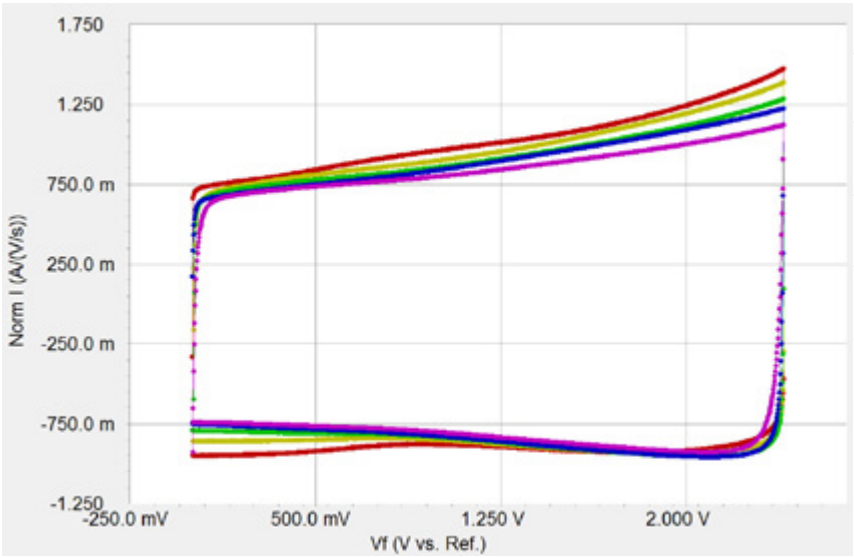


Figure 8. CV for a Taiyo Yuden pseudo-capacitor, normalized to scan rate. Red is the fastest scan rate; purple is the slowest.

Electrochemical Impedance Spectroscopy

Electrochemical Impedance Spectroscopy (EIS) is the preferred method for measuring ESR of super-capacitors. EIS also can measure capacitance and capacitor non-ideality. For basic information on EIS, see Gamry's application note at www.gamry.com:

"Basics of Electrochemical Impedance Spectroscopy"

EIS Model for a Super-capacitor

The most common model fitted to super-capacitor EIS spectra is a simplified Randles model:

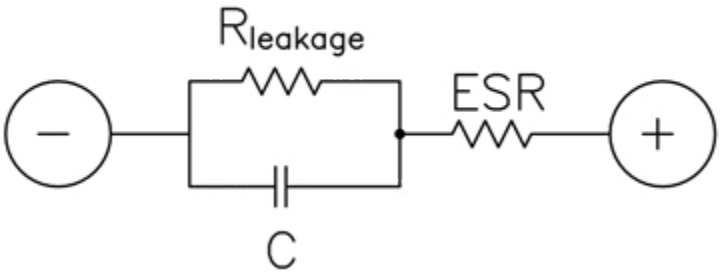


Figure 9. Randles equivalent circuit for modeling super-capacitors.

The elements in the model are:

C	Ideal capacitance
ESR	Equivalent Series Resistance
$R_{leakage}$	Leakage resistance

The values used to plot Figure 10 were chosen to approximate those of a typical EDLC device. The EIS magnitude is shown as circles, and the phase is shown as crosses.

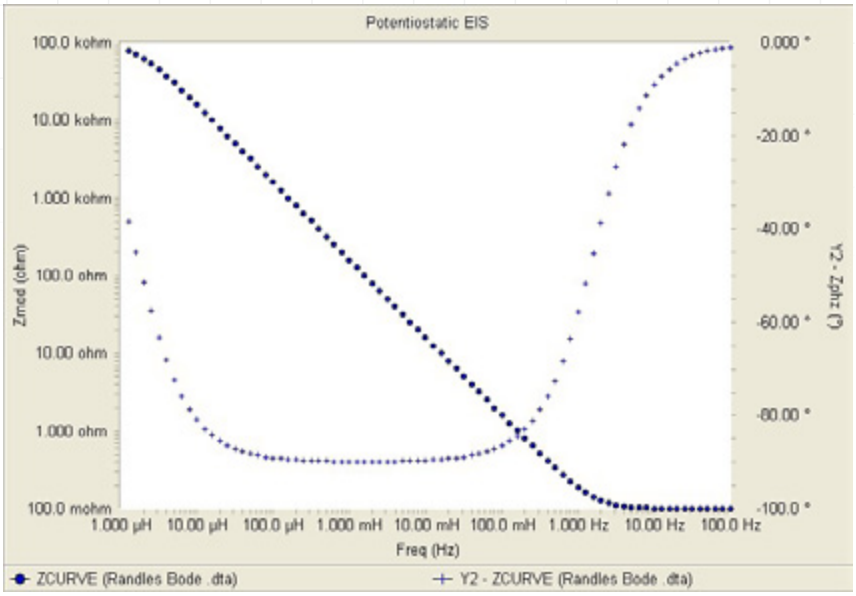


Figure 10. Ideal Bode plot of the equivalent circuit in Figure 8, with C = 1 F, ESR = 100 mΩ, and $R_{leakage}$ = 100 kΩ.

The Bode spectrum in Figure 10 has three regions:

- Above 10 Hz the magnitude and phase approach 100 mΩ and 0°. ESR dominates this region.
- In the region between 100 μHz and 10 Hz, capacitance controls the impedance. Magnitude-versus-frequency is linear (on the log-log Bode plot) with a slope of –1 and the phase approaches –90°.
- Below 10 μHz, the impedance begins a transition back towards resistive behavior as leakage resistance becomes dominant. This transition is incomplete, even at 1 μHz. EIS spectra of real devices rarely give much information about leakage resistance, because its effects are seen at impractically low frequencies.

EIS Measurement Mode

Gamry's Electrochemical Impedance Spectroscopy software can measure EIS using three different control modes:

- Potentiostatic EIS
- Galvanostatic EIS
- Hybrid EIS

Potentiostatic and galvanostatic modes control cell voltage and current respectively. Hybrid mode uses galvanostatic cell control, but changes the AC current to maintain a fixed AC-voltage response.

Galvanostatic and hybrid mode EIS are preferred for very-low-impedance cells, where small errors in the DC voltage can create huge DC currents.

The impedance of the 3 F capacitors used to generate data for this white paper is high enough that any mode of control may be used. Potentiostatic mode is the most common EIS mode, so this mode was chosen.

EIS Spectra on a 3 F EDLC at Different Potentials

Figure 11 is a Bode plot of EIS spectra of a 3 F EDLC recorded at three DC potentials: 0.0, 1.25 and 2.50 V (in blue, green and red). The capacitor was held at the DC voltage for 10 min between spectral acquisitions. The spectra were measured potentiostatically with an AC voltage of 1 mV RMS.

The Gamry ***Sequence Wizard*** was also used to record these data. The loop contained both an equilibration step and EIS data-acquisition.

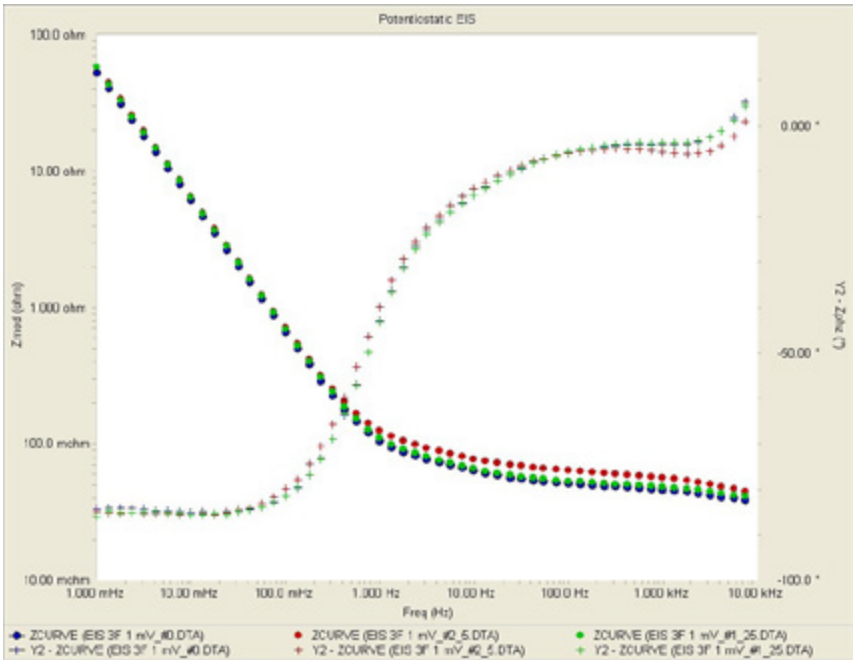


Figure 11. Bode plot of 3 F EDLC at 0.0 V (blue), 1.25 V (green), and 2.50 V (red).

These spectra differ significantly from the ideal in the previous section. Differences include:

- No sign of the leakage resistance in this frequency range.
- Phase between 1 Hz and 100 Hz never approaches the simple model's 0° prediction.

The spectrum of an ideal capacitor is independent of DC voltage. Obviously, the EDLC characterized by these spectra shows non-ideality from 1 Hz to 10 kHz.

Fitting a Model to the Spectrum

The impedance spectrum in Figure 12 was measured on a 3 F EDLC held at 2.25 V. The data were recorded with a 1 mV excitation and potentiostatic cell control. The green lines on this graph are a modified Randles-model fit to the data. The fit parameters are:

C 2.51 F ± 12 mF

ESR 62 mΩ ± 314 $\mu\Omega$

$R_{leakage}$ 773 Ω ± 59 Ω

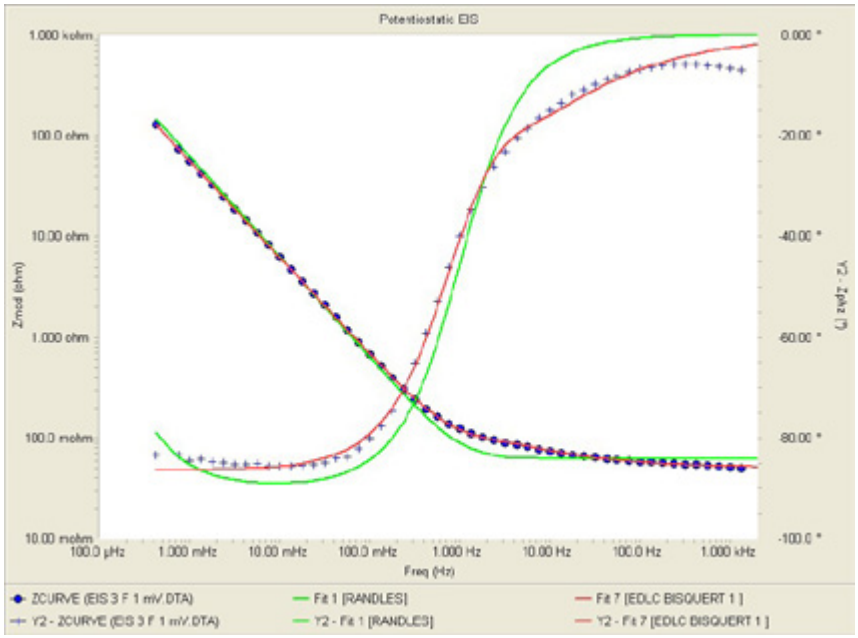


Figure 12. Bode plot of 3 F EDLC at 2.25 V, with Randles model fit (green solid line) and porous-electrode with transmission-line fit (solid red line).

The agreement in Figure 12 between the Randles model and the spectrum is poor. This is typical of EIS on EDLC capacitors where electrode porosity leads to very non-uniform access of the electrolyte to the electrode surface, so Faradaic reactions occur. Simple resistor-and-capacitor models do not apply.

The fit to the data is much better using a porous-electrode, transmission-line model when a Bisquert open element is used (Figure 13).

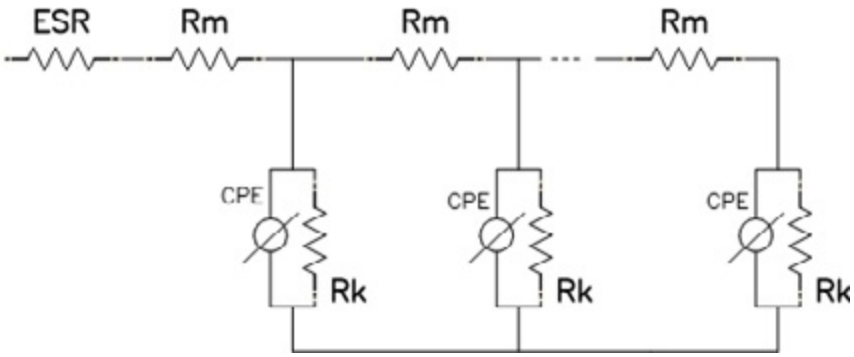


Figure 13. Porous-electrode, transmission-line model used in Figure 12 modeling.

The fit is in red in Figure 13. The fit parameters are:

R_m	112 mΩ ± 22 mΩ
R_k	2.2×10^{30} Ω ± 1×10^{38} Ω
Y_m (CPE)	2.3 S·s/A ± 0.15 S·s/A
α (CPE)	0.960 ± 0.033
ESR	50×10^{-3} Ω ± 639×10^{-6} Ω

For an explanation of the model, see this application note at www.gamry.com:

"Demystifying Transmissions Lines: What are they? Why are they Useful?"

The high uncertainty in R_k is expected. The spectrum does not include frequencies where R_k affects the impedance.

EIS Spectrum of a Low-ESR 650 F EDLC

EIS measurement on very-low-ESR capacitors is difficult. It generally requires:

- True four-terminal measurements
- Galvanostatic cell control
- Low-resistance contacts
- Twisted-pair or coaxial cell leads

Two of Gamry's application notes give suggestions for making low-impedance EIS measurements:

"Accuracy Contour Plots"

"Verification of Low-impedance EIS Using a 1 mΩ Resistor"

EIS spectra were recorded on a Maxwell[4] capacitor (part #BCAP0650 P270). This 650 F capacitor was rated for ESR less than 600 $\mu\Omega$ at 1 kHz.

Figure 14 is a photograph that shows the connections used to record the EIS spectrum of this device. Connections were made with 1.5 mm-thick copper sheet. The current-carrying leads and voltage-sensing leads are on opposite sides of the device.

Figure 14. Connections from the potentiostat to the Maxwell capacitor.

Warning: Avoid shorting capacitor terminals though low-resistance connections. Very dangerous currents of hundreds or even thousands of ampères could flow.

The EIS spectrum is presented in Figure 15. This spectrum was recorded in Hybrid Mode with a 1 mV AC voltage. The impedance at 1 kHz is 335 $\mu\Omega$, which is less than this capacitor's rated ESR of 600 $\mu\Omega$.

4. Maxwell Technologies, Inc., 3888 Calle Fortunada, San Diego, CA 92123.

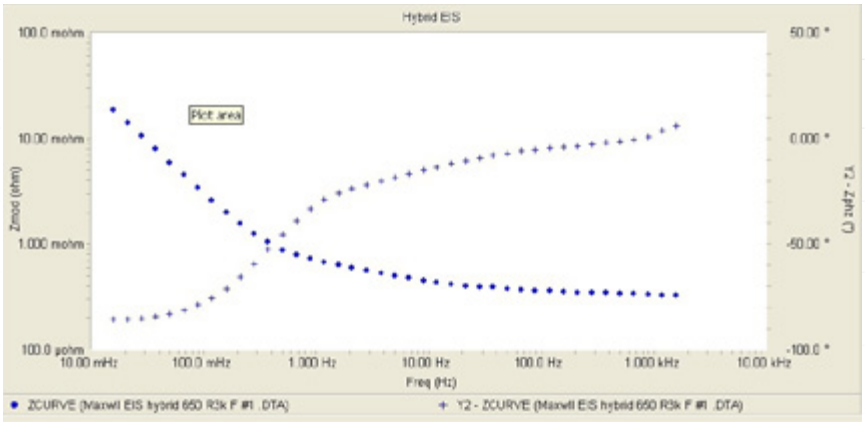


Figure 15. EIS from 650 F EDLC.

EIS on a Pseudo-capacitor

EIS spectra recorded on an ideal capacitor at different DC voltages should superimpose.

EIS confirms the voltage dependence of measured capacitance on a PAS pseudo-capacitor. This is the same capacitor used previously for CV testing. EIS spectra were recorded at DC voltages of 0, 1.2, and 2.4 V (Figure 16). Unlike the EDLC case, low-frequency impedance was different at each voltage.

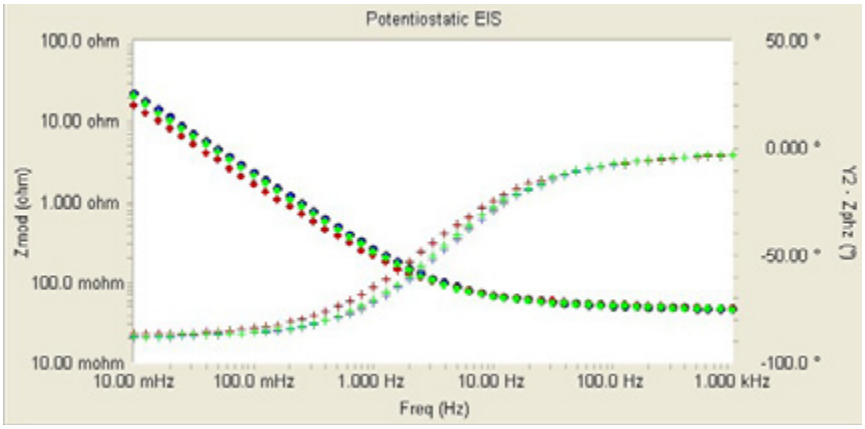


Figure 16. EIS for a PAS pseudo-capacitor at 0 (blue), 1.2 (green), and 2.4 V (red).

In the simple Randles model, capacitance controls the impedance at the lowest frequencies in the graph above. In the plot above, impedance in this region depends on DC voltage, so the capacitance must also depend on DC voltage.

Measurement of Leakage Current

Leakage current can be measured in at least two ways:

- Apply a DC voltage to a capacitor and measure the current required to maintain that voltage.
- Charge a capacitor to a fixed voltage, then open the circuit on the capacitor and measure the voltage change during self-discharge.

Conway's book includes a chapter that discusses leakage current and self-discharge of super-capacitors.

In an attempt to make the specifications of a super-capacitor look good, some manufacturers specify that leakage current is measured after 72 hours with voltage applied. Under these conditions, leakage current can be as low as 1 μA/F.

Direct Measurement of Leakage Current

Direct potentiostatic measurement of capacitor leakage current is quite challenging. The test must apply a DC potential to capacitor under test, and measure extremely small currents.

Typically, capacitor charging currents are in ampères and leakage currents are in microampères, a range of 10^6. Noise or drift in the DC potential can create currents that are larger than the leakage current.

For example, assume the 3 F capacitors used in our testing have an ESR of 100 mΩ. We want to measure a leakage current of 1 μA on these: we'd like current noise to be less than the 1 μA signal.

At frequencies where ESR is the dominant impedance, 0.1 μV of noise in the applied voltage will create a noise current of 1.0 μA. At lower frequencies, where our 3 F capacitance dominates the impedance, a voltage drift of 0.3 μV/s creates a current of 1.0 μA.

Fast acquisition of data, external noise sources, or lack of a Faraday cage can lead to large apparent DC currents or continual switching between current ranges.

The Potentiostatic test in Gamry's Electrochemical Energy Software will not accurately measure leakage current, for it only offers a dynamic range of about 10^4.

PWR800 Leakage-current Measurement

Figure 17 presents leakage current measured on a new 3 F capacitor. The plot is logarithm of current versus time for five days at 2.5 V.

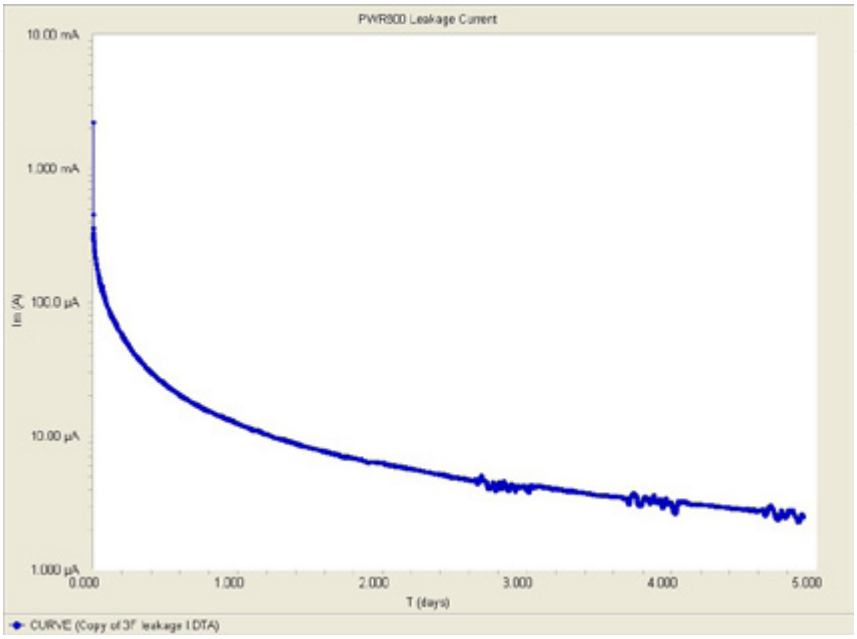


Figure 17. Leakage current vs. time for a 3 F capacitor.

Note that current is still falling five days after application of the potential. The manufacturer specifies leakage current on this capacitor at less than 5 μA after 72 hours; the measured value was about 3.2 μA.

The data in this plot were smoothed using a Savitsky-Golay algorithm with a 60 s window. The periodic noise signal is caused by daytime air-conditioning.

A special script has been developed for direct leakage-current measurement using the Electrochemical Energy tools. This script is named:

PWRLeakageCurrent.exp

Unlike the potentiostatic technique, this script applies a voltage using the instrument's potentiostat mode and measures leakage current.

It uses a user-entered estimate for ESR to avoid I/E Converter ranges where voltage noise can overload the current measurement circuitry. A gain of 10 in the current measurement allows measurement with ten times greater voltage noise and drift.

Measurement of Self-discharge

Self-discharge causes the open-circuit voltage of a charged capacitor to decrease over time. During self-discharge, leakage current discharges the capacitor, even though there is no external electrical current.

Conway's book describes three mechanisms for self-discharge. These mechanisms can be distinguished by analyzing the shapes in voltage-versus-time curves recorded over long periods of time. This analysis was not done on the data presented here.

Instantaneous leakage current, I_{leak}, can be calculated by multiplying the rate of voltage-change during self-discharge by capacitance.

$$I_{\text{leak}} = C\frac{dV}{dt} \qquad \text{Eq.10}$$

The graph in Figure 18 is the open-circuit voltage-versus-time curve of a 3 F capacitor left open-circuit after 12 hours at 2.5 V. This was recorded with the capacitor pre-charged to 2.5 V in the previous test. The voltage change was less than 2 mV after 30 min.

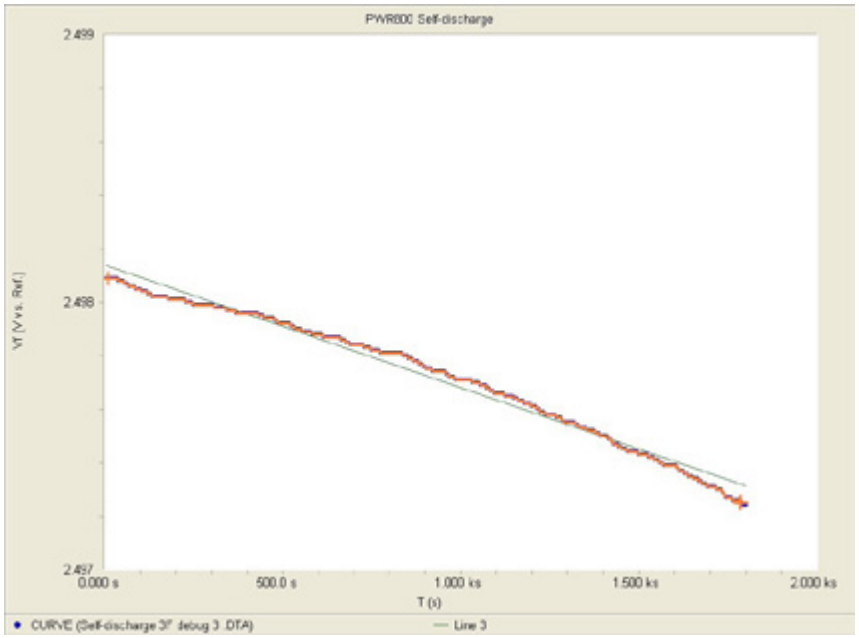


Figure 18. Voltage-decay with time of a 3 F capacitor, after 12 h charge to 2.5 V.

The red line on the graph is a linear-least-squares fit of the voltage-decay data. The slope is 0.55 μV/s.

The leakage current is

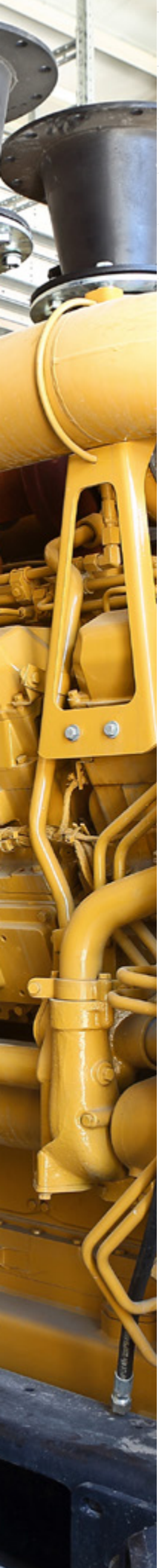
$$I_{\text{leak}} = C\frac{dV}{dt} = 3\ \text{F} \cdot \frac{0.55\ \mu\text{V}}{\text{s}} = 1.6\ \mu\text{A} \quad \text{Eq.11}$$

The slope calculation used the ***Linear Fit*** function in Gamry's Echem Analyst.

The Electrochemical Energy package has added a script that makes this measurement. This script is named:

PWR_SelfDischarge.exp

It applies a constant potential for a user-requested length of time. It then turns off the cell and measures changes in open-circuit voltage. The instrument's offset and gain circuitry allows measurement of very small voltage-differences.



Part 2: Cyclic Charge-Discharge and Stacks

Introduction

This application note is the second in a three-part series describing electrochemical techniques for energy-storage devices. It explains Gamry's PWR800 measurement software and describes techniques to investigate electrochemical capacitors. This application note can also be extended to testing batteries.

An introduction to electrochemical capacitors is found in Part 1 of this application note, which discusses techniques familiar to chemists who have worked outside of energy-storage applications. Part 3 describes theory and practice of EIS measurements on capacitors.

You can find all parts of this application note in the Application Notes section on Gamry's homepage, www.gamry.com.

Experimental

The data shown in this note were recorded on a Gamry Instruments potentiostat using Electrochemical Energy software. Tests were run with commercial 3 F (P/N ESHSR-0003C0-002R7) and 5 F (P/N ESHSR-0005C0-002R7) electric double-layer capacitors (EDLCs) from Nesscap[5]. EDLCs exhibit much lower charge and discharge times than batteries, reducing dramatically the time for measurements.

Basics of Cyclic Charge-Discharge

Cyclic Charge-Discharge (CCD) is the standard technique used to test the performance and cycle-life of EDLCs and batteries. A repetitive loop of charging and discharging is called a cycle.

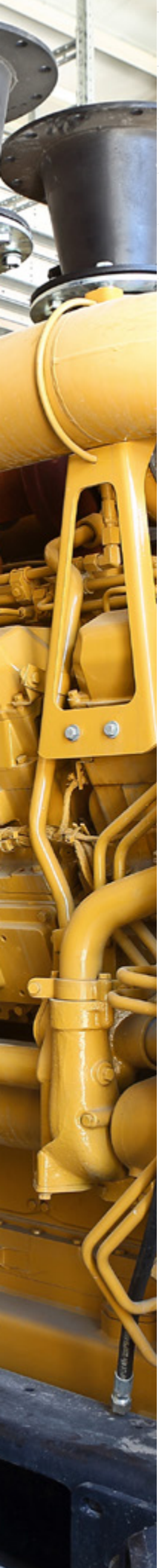
Most often, charge and discharge are conducted at constant current until a set voltage is reached. The charge (capacity) of each cycle is measured and the capacitance *C*, in farads (F), is calculated (Eq. 12).

$$C = \frac{Q}{V} \quad \text{Eq. 12}$$

where *Q* is the charge in coulombs, and *V* is the voltage window. Both are plotted as a function of cycle number. This curve is called the *capacity curve*.

In practice, charge is commonly called capacity. Usually, capacity has the unit of ampere-hour (Ah), where 1 Ah = 3600 coulombs.

5. Nesscap Energy Inc., 24040 Camino Del Avion #A118, Monarch Beach, CA 92629.



If capacity falls by a set value (10% or 20% is customary), the actual number of cycles indicates the cycle-life of the capacitor. In general, commercial capacitors can be cycled for hundreds of thousands of cycles.

Figure 19 shows CCD data recorded on a new 3 F EDLC. Five cycles are shown with current and voltage plotted versus time, with each cycle graphed in a different color.

The lighter-colored waveform is the current applied to the capacitor. The darker-colored waveform shows the measured voltage. The capacitor was cycled between 0 V and 2.7 V with a current of ±0.225 A.

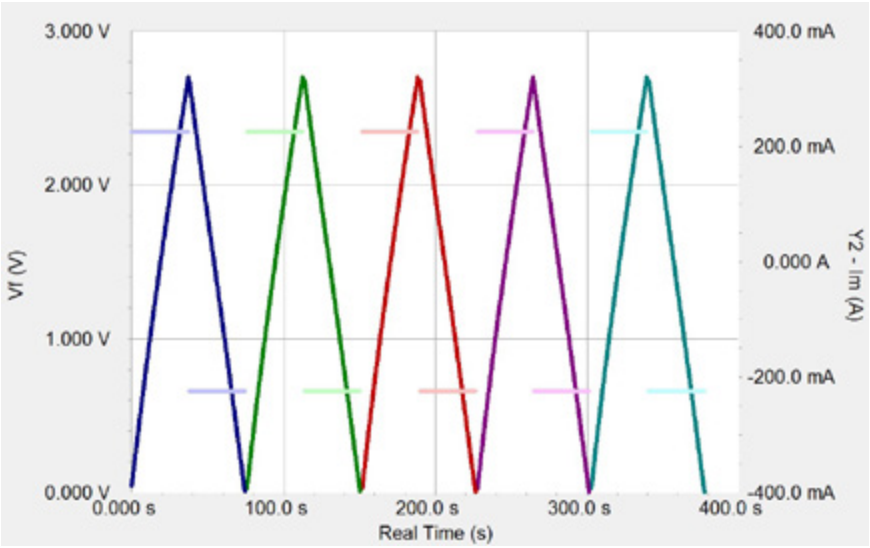


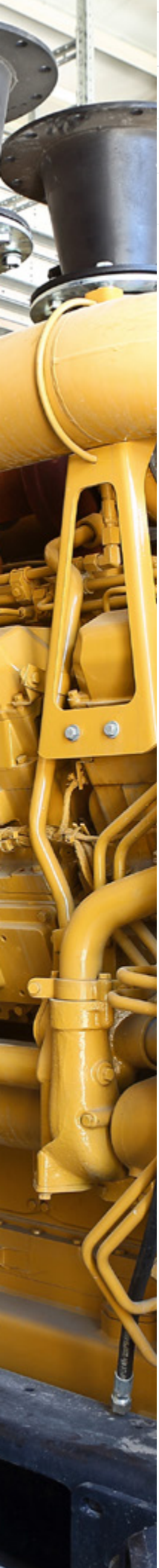
Figure 19. CCD test on a new 3 F EDLC. Voltage and current versus time are shown for five cycles. For details, see text.

This new EDLC shows almost ideal behavior: the slope of the curve (*dV/dt*) is constant and is defined by Eq. 13.

$$\frac{dV}{dt} = \frac{I}{C} \qquad \text{Eq. 13}$$

V is the cell potential in volt (V), I is the cell current in ampere (A), and *Q* is the charge in coulomb (C) or ampere-second (A·s).

Figure 20 shows the same CCD procedure but on a 3 F capacitor damaged by excessive voltage. This capacitor's behavior is obviously far from ideal.



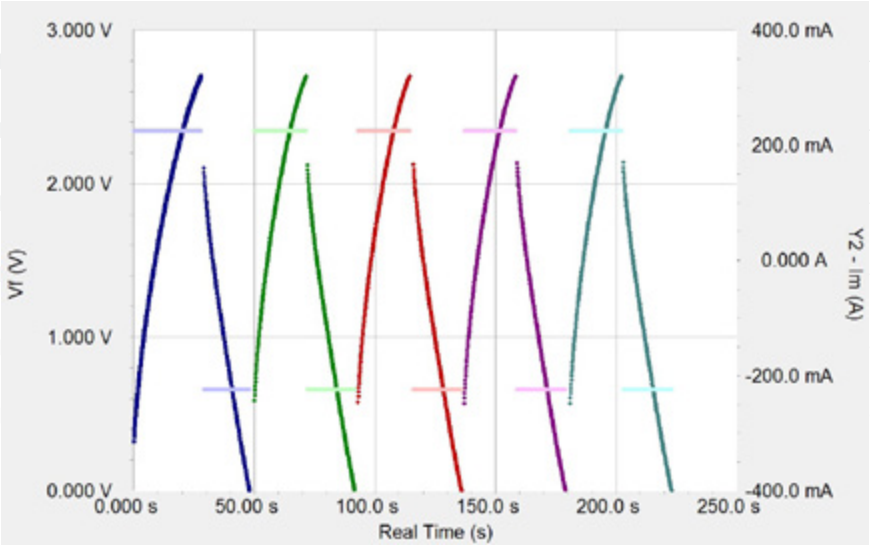


Figure 20. CCD test on a damaged 3 F EDLC. Voltage and current versus time are shown for five cycles. For details, see text.

Increased self-discharge causes an exponential shape of charge and discharge voltage versus time. A higher equivalent series resistance (ESR) also leads to a large voltage drop (IR-drop) at each half-cycle, which dramatically reduces power and capacity. The damage has greatly decreased the efficiency of this EDLC.

Gamry's Cyclic Charge-discharge Software

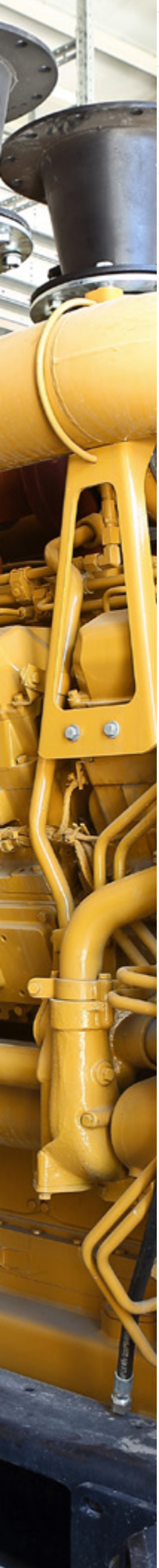
Figures 19 and 20 showed individual charge and discharge curves. More commonly, CCD data are plotted as a capacity curve: capacity versus cycle number.

Gamry's CCD data file contains additional information that allows plotting Δ capacity, energy, energy efficiency, Coulombic efficiency, and capacitance versus cycle number.

Figure 21 shows the typical setup windows for a CCD experiment, presented in three pages. A simple CCD test consists of a repetitive loop through several steps:

1. Constant current charge
2. Potentiostatic hold (optional)
3. Rest at open-circuit potential (OCP) (optional)
4. Constant-current discharge
5. Rest at OCP (optional)

On ***Page 1*** of the setup, output file name as well as various cell and setup parameters can be defined. The ***Working Lead*** parameter specifies how the potentiostat is connected to a cell. When the working lead (green) is connected to the positive electrode (discharge cathode) of the electrochemical cell, select the Positive radio button for this parameter. Otherwise, select the Negative radio button for this parameter.



The optional ***Cable Check*** warns in a separate window how cable connections are appropriate for the selected ***Cell Type***.

Please refer to Gamry's ***Help*** menu for a detailed description of all setup parameters.

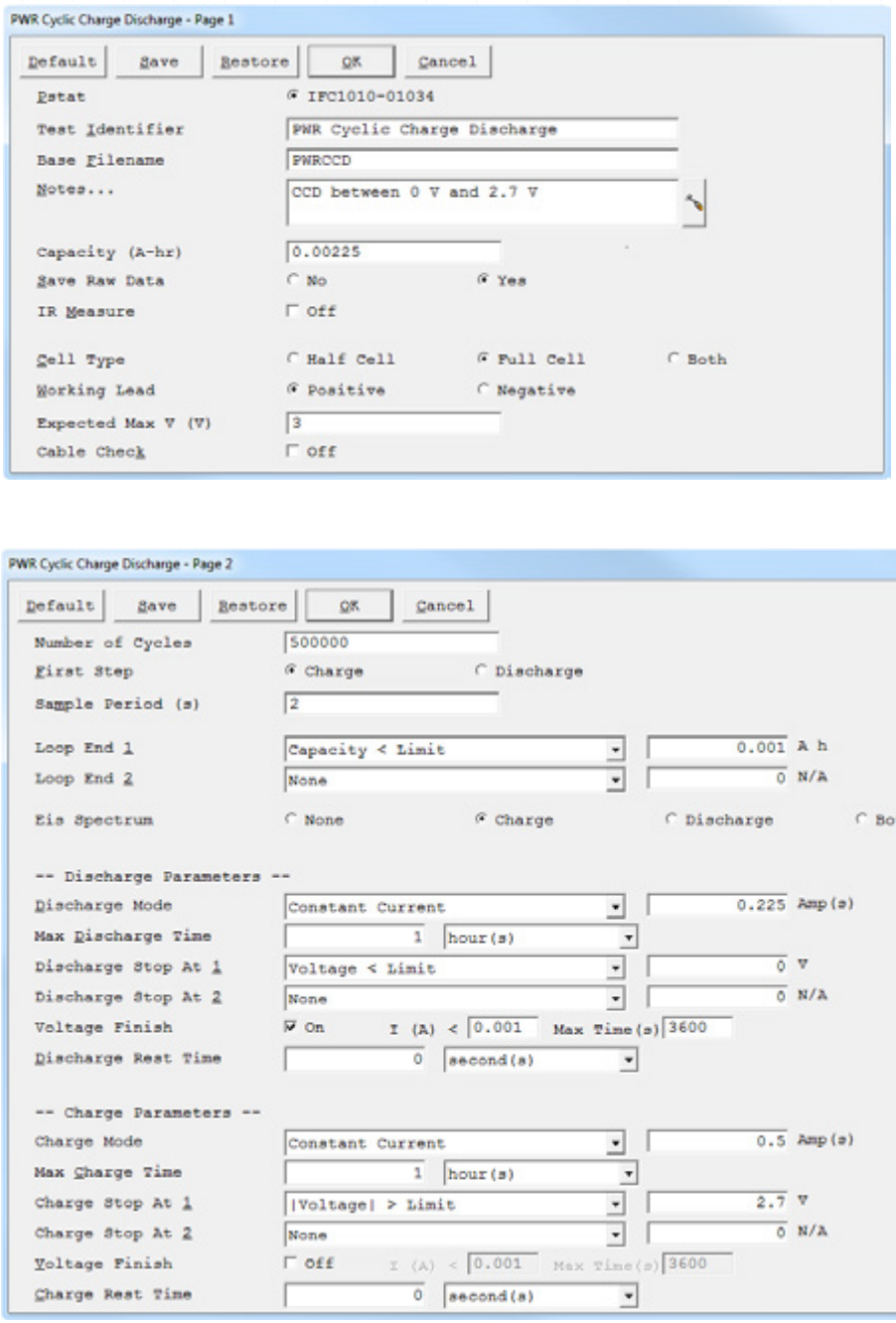
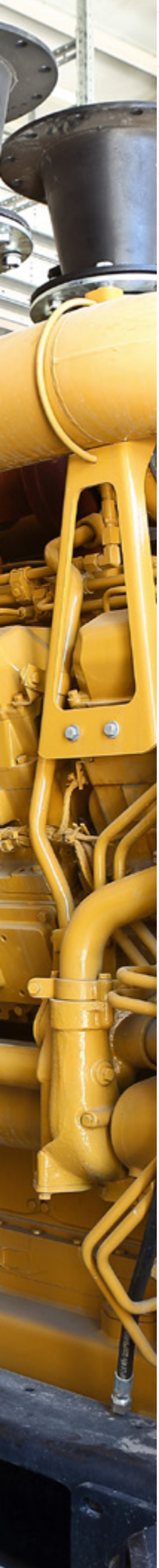
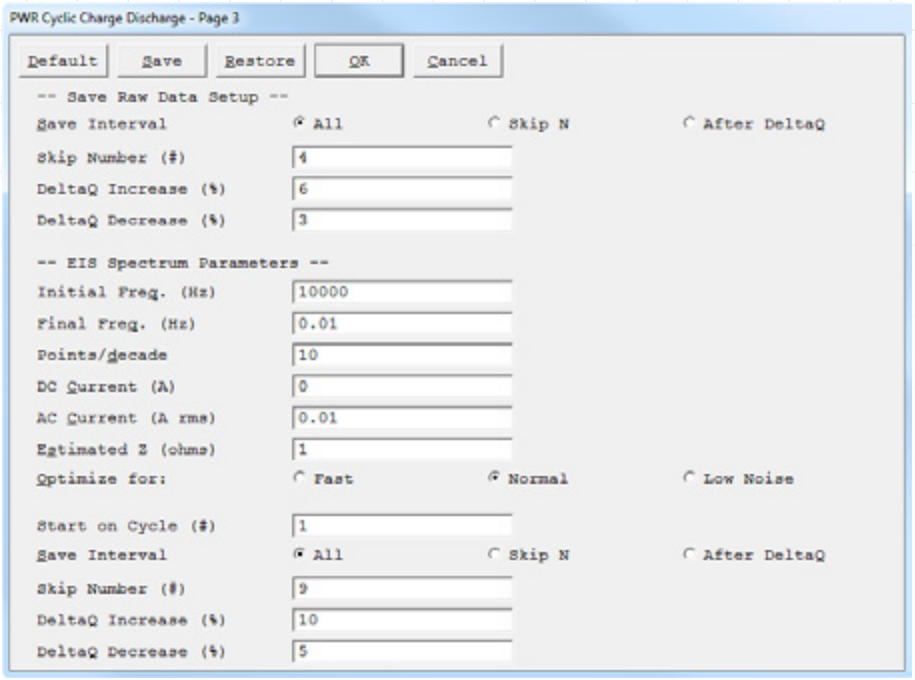


Figure 21. Software setup for a CCD experiment.





The Reference 3000 with an Auxiliary Electrometer allows measuring the voltage of up to eight cells in a serially connected stack individually. If connected, an optional parameter appears in the setup window. This parameter consists of checkboxes to select which channels are active during an experiment.

All relevant parameters for the charge and discharge steps are set on ***Page 2*** of the CCD setup (see Figure 21).

A CCD experiment can be started with a charge or discharge step. The length of a CCD test can be controlled by the cycle number and various Loop End criteria (see Figure 22). The measurement stops after reaching the cycle limit, a loop end criterion, or it may be cancelled at any time by pressing F1–Abort.

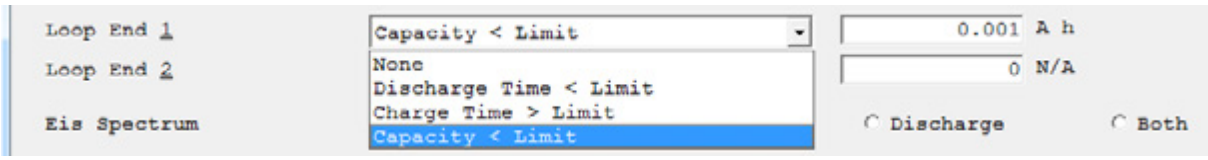
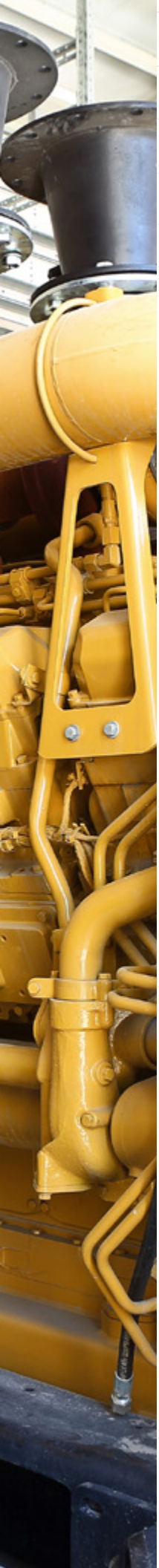


Figure 22. Selectable Loop End criteria which can terminate a CCD experiment prematurely.



The individual length of a charge/discharge step can be further controlled by setting a maximum time or various stop criteria (see Figure 23). Stop criteria can be defined by the cell's voltage, temperature behavior, charge, or energy. A charge/discharge step is terminated prematurely if any of the set criteria is met. The CCD experiment continues then with the next step.

After each single step, the cell's capacity is automatically calculated and shown in a capacity curve.

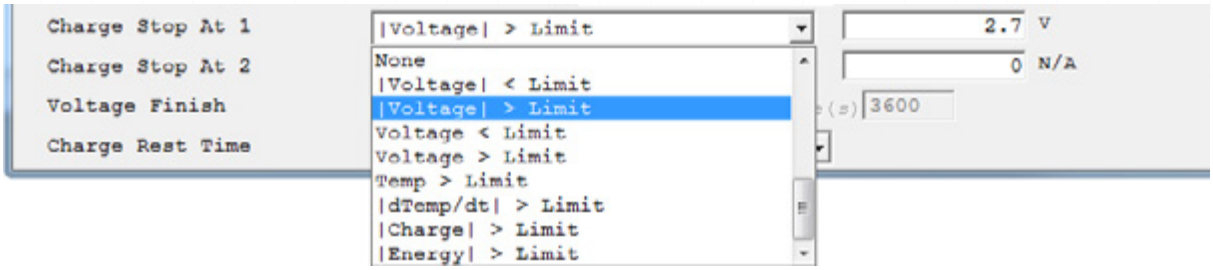


Figure 23. Selectable charge/discharge Stop criteria.

The discharge step allows four different modes: ***Constant Current, Constant Power, Constant Load, or Constant C rate (Capacity * N, Capacity / N)*** (see Figure 24). Please note that the charge step can be only performed in Constant Current mode for CCD experiments. However, single charge experiments can be also performed in Constant C-rate mode.

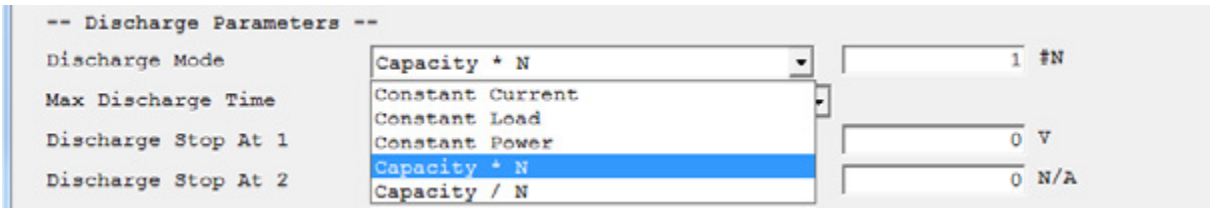
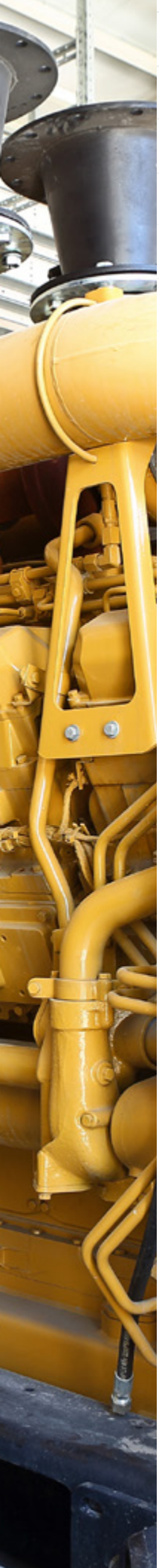


Figure 24. Selectable modes for the discharge step (Constant C rate mode is shown).

The C rate (charge or discharge rate) defines how fast a battery is charged or discharged. In general, the capacity of a battery is rated at 1C. This means that a battery with a capacity of 1 Ah provides a current of 1 A for one hour. Higher C rates provide larger current but for a shorter period.



Two parameters are crucial when selecting Constant C rate mode. The first parameter is the rated/expected capacity of the battery and is set in the first setup window of a CCD experiment. The second parameter is the multiplier/divisor N and defines the rate. Note that ***N*** is an integer. Use ***Capacity **** N for C-rates above 1C and ***Capacity / N*** below 1C.

Enabling ***Voltage Finish*** holds the cell potentiostatically at the end potential until the measured current falls below a limiting value or a set time is reached. This step is especially advisable if (optional) EIS experiments are performed as it ensures that the potential remains stable and does not drift.

The corresponding EIS parameters can be set on ***Page 3*** of the CCD setup. In addition, the save intervals for raw data (individual charge and discharge curves) as well as impedance data can be selected.

CCD on Single 3 F EDLCs

Different voltage limits

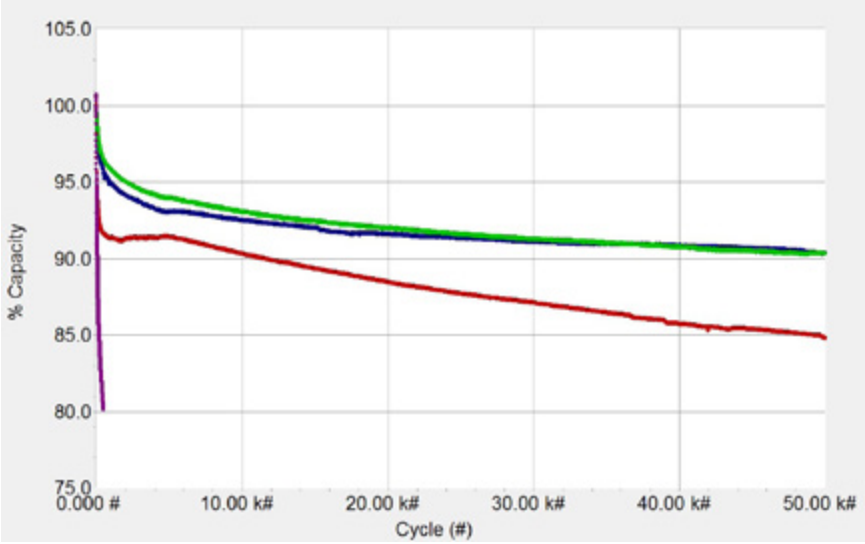


Figure 25. Percentage change of capacity of a 3 F EDLC during cycling to different voltage limits. (●) 2.7 V, (●) 3.1 V, (●) 3.5 V, (●) 4.0 V.

Cycle-life depends on a number of variables:

- Limiting voltage,
- Current used for charge and discharge,
- Temperature

To demonstrate the first point, four 3 F EDLCs were cycled to different voltage limits, most of them well beyond the 2.7 V maximum voltage specified for the EDLC.

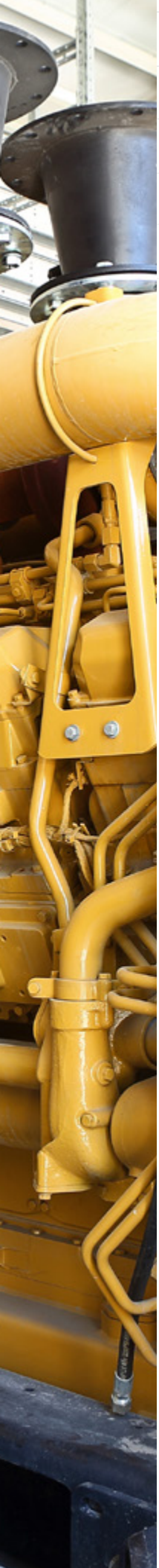


Figure 25 shows the corresponding curves with the relative change of capacity for up to 50 000 cycles. The capacitors were charged and discharged with a current of ±2.25 A. The lower voltage limit was 1.35 V, which is the half-rated voltage of the EDLC. The upper voltage limits were set to 2.7 V, 3.1 V, 3.5 V, and 4.0 V.

Capacity-fade is more pronounced on the samples charged to higher voltage limits. The capacity is reduced by only 10% after 50 000 cycles at potentials below 3.0 V. The capacitor charged to 4.0 V lost 20% of its capacity after 500 cycles.

The strong degradation in performance at higher potentials mainly occurs when Faradaic electrochemical reactions decompose the electrolyte. This can inhibit the electrode surface, lead to gas formation, damage the electrodes, and have other adverse effects.

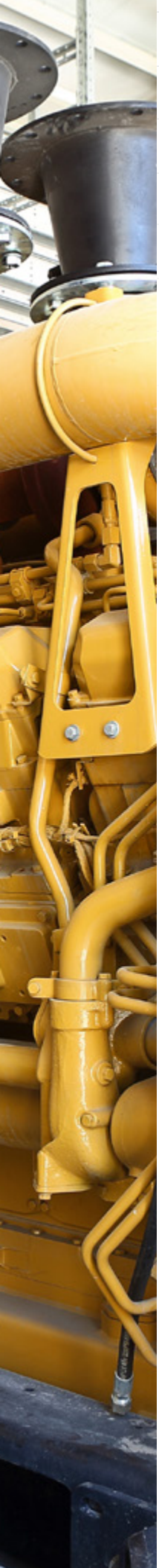
Different charge- and discharge-currents

Cycle-life also depends on the applied current. To demonstrate the effect of higher currents on CCD experiments, current values significantly beyond the specifications of the capacitor were chosen. The used 3 F capacitors used are specified for currents of 3.3 A.

For these experiments currents larger than 3 A were needed. This requires the use of a Gamry Instruments Reference 30k Booster.

The Reference 30k Booster is an extension for the Reference 3000, with a compliance current expanded to ±30 A. It works with all applications for the Reference 3000, including the Auxiliary Electrometer. For more information, visit Gamry's website: ***www.gamry.com***

Three capacity plots with different charge and discharge currents are shown in Figure 26. The EDLCs were charged and discharged between 1.35 V and 3.5 V. The applied current was set to 2.25 A, 7.5 A, and 15 A.



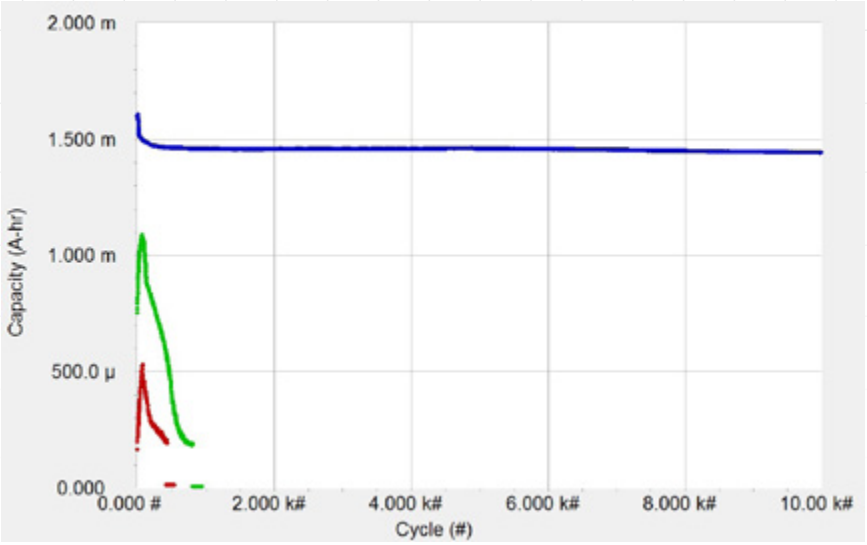


Figure 26. Capacity curves of a 3 F EDLC during cycling with different currents. (●) 2.25 A, (●) 7.5 A, (●) 15 A.

The capacity curves at higher currents show a steep capacity decline with increasing cycle number. The two EDLCs that were cycled with 7.5 A and 15 A failed before reaching 400 and 800 cycles respectively.

The capacity curves at higher currents show a steep capacity decline with increasing cycle number. The two EDLCs that were cycled with 7.5 A and 15 A failed before reaching 400 and 800 cycles respectively.

Even on the first CCD cycle, higher currents lead to reduced capacity. Voltage is lost due to IR-drop (VLoss) according to Eq.14:

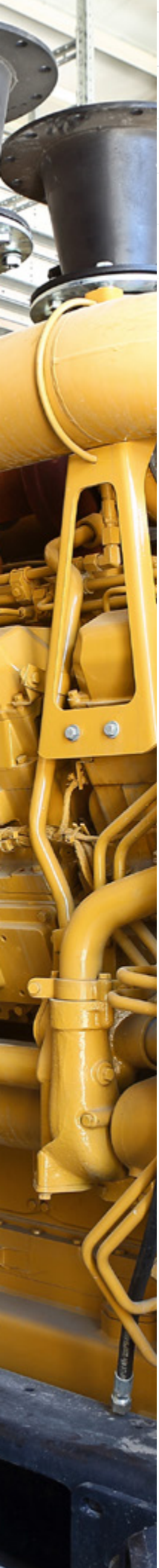
$$V_{Loss} = 1 \cdot ESR \qquad \text{Eq.14}$$

The *IR*-drop voltage is not useful in charging and discharging the capacitor. Both charge and discharge have their effective voltage range V_{eff} reduced by twice the *IR*-drop voltage.

Assuming 40 mΩ ESR for 3 F capacitors, we expect these parameters for different currents:

I (A)	V_{Loss} (V)	V_{eff} (V)]	Q (mAh)	P_{Loss} (W)
2.25	0.09	1.97	1.6	0.2
7.5	0.3	1.55	1.3	2.3
15	0.6	0.95	0.8	9.0

Table 1. Estimated IR-drop voltage, effective voltage range, capacity, and power loss for 3 F EDLCs with 40 mΩ ESR. For details, see text.



The IR-drop reduces capacity by about 19% and 50% respectively. Note the rough agreement between the initial capacities of the measurements with 7.5 A and 15 A in Figure 26 and Table 1.

The two capacitors cycled with 7.5 A and 15 A got quite hot before they failed.

The heat generated by rapid cycling is also caused by IR-losses. Assuming a constant ESR, the power loss PLoss in these devices can be estimated from Eq.14:

$$P_{Loss} = I^2 \cdot \mathrm{ESR} \qquad \text{Eq.14}$$

Table 1 shows that power loss is estimated to be greater than 2 W, even at 7.5 A. The small 3 F capacitors used for these tests cannot dissipate this much power without getting very hot. Heat can cause degradation of the electrolyte and dramatically reduce lifetime.

The capacitor cycled at 15 A was so badly swollen at the end of the test that it was surprising it had not burst.

CCD on Stacks for Higher Voltages

Balanced stack

For high-power applications, several energy-storage devices are often combined in serial and parallel circuits. For serially-connected capacitors, Eqs. 15 and 16 apply:

$$\frac{1}{C} = \sum_{i=1}^{n} \frac{1}{C_i} \qquad \text{Eq.15}$$

$$V = \sum_{i=1}^{n} V_i \qquad \text{Eq.16}$$

The total capacity for n identical capacitors is the n^{th} fraction of the capacity of a single capacitor. The individual voltages of the capacitors are summed to give the total voltage of the stack.

Figure 27 shows a schematic diagram for a serially connected stack of capacitors.

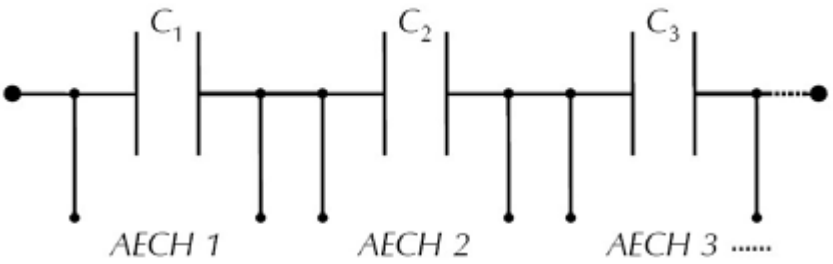
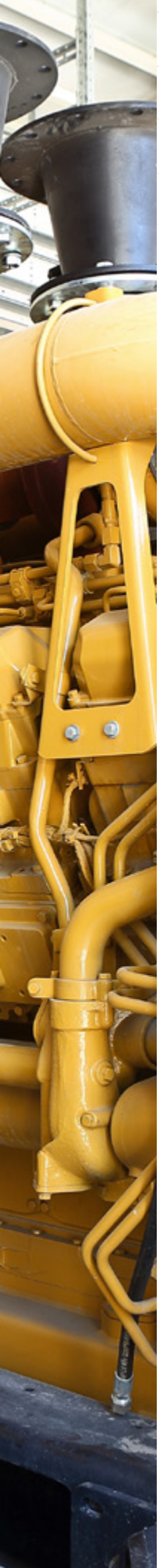


Figure 27. Diagram of serially-connected capacitors with Auxiliary Electrometer connections.



If all single cells in a stack show the same parameters, the stack is called balanced. The stack is unbalanced if there are cells that differ in performance parameters like capacitance, ESR, or leakage resistance.

Gamry's Auxiliary Electrometer (AE) enables detailed investigation of single cells in a stack. Each individual channel (AECH 1, AECH 2, AECH 3,...) measures the voltage across a cell.

Capacity curves cannot show irregularities in stacks. All cells receive the same current so their capacities are identical. In the following sections, tests were done with small stacks containing three series-connected EDLCs. The stacks were deliberately unbalanced to show the effect of two common irregularities. To reveal these irregularities, different plots were used.

Unbalanced stack with different capacitances

Using capacitors with different capacitances in a stack leads to fluctuations in voltage defined by Equation 17.

$$V_i = \frac{Q}{C_i} \qquad \text{Eq.17}$$

Applying a constant charge Q on a stack leads to a lower voltage Vi for single cells with higher capacitance C_i.

A serial stack made up of two 3 F EDLCs (C_1, C_2) and one 5 F EDLC (C_3) (see also Figure 28) was used to test an unbalanced stack. All three capacitors were initially charged to 1.35 V before being added to the stack, so the initial stack voltage was close to 4 V.

The stack was cycled for 500 cycles with a current of ±0.225 A. The test started with a charge step. The cycle limits were set to 4 V and 9.5 V. The voltage of each single cell was measured with three AE channels.

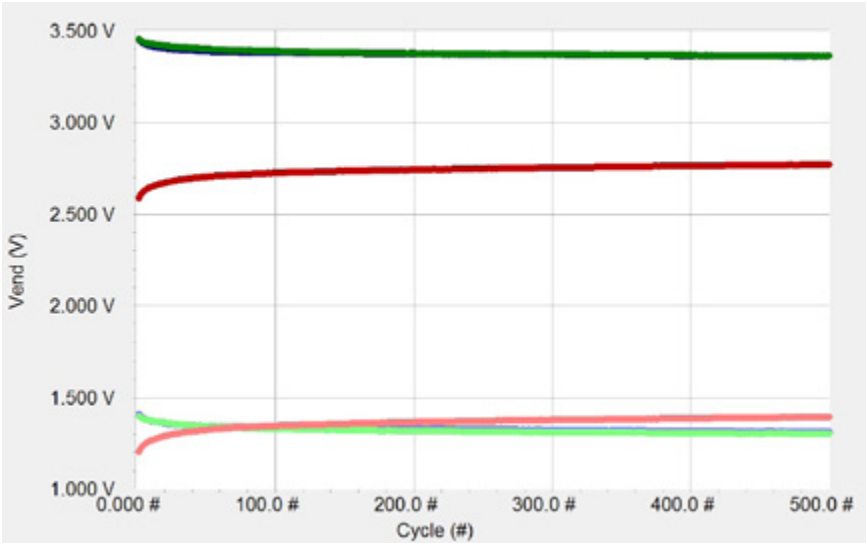


Figure 28. Limiting potentials for the charge (darker) and discharge process (lighter) of an unbalanced stack with two 3 F EDLCs (● C_1, ● C_2) and one 5 F EDLC (● C_3).

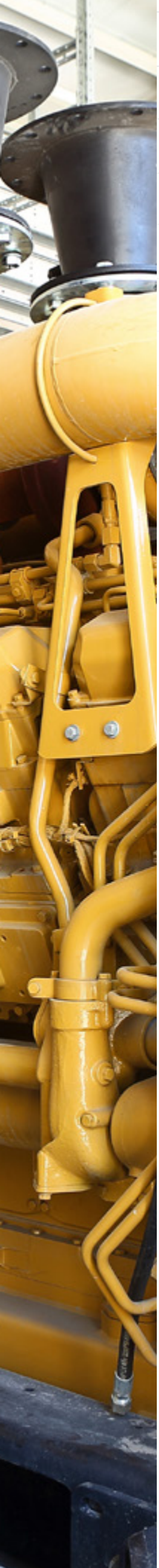


Figure 28 shows one presentation of the data from this test. The limiting voltages of each channel for the charge (darker colored) and discharge step (lighter colored) versus cycle number are plotted.

As expected, the final discharge voltage for each cell (regardless of capacitance) is close to 1.3 V. The small deviations from 1.3 V are probably caused by leakage-current imbalance, described later.

The final charge voltage is more interesting. If we had a balanced stack, the fully charged stack voltage of 9.5 V would be evenly divided among the cells so each cell would charge to about 3.16 V.

The 3 F EDLCs (C_1 and C_2) are charged to about 3.36 V in the unbalanced stack. Each is overcharged by about 200 mV. The 5 F capacitor (C_3) is only charged to about 2.7 V and therefore undercharged by 400 mV. The voltage imbalance is independent of the cycle number.

Figure 29 shows the calculated energy of the charge step versus cycle number for the same measurement.

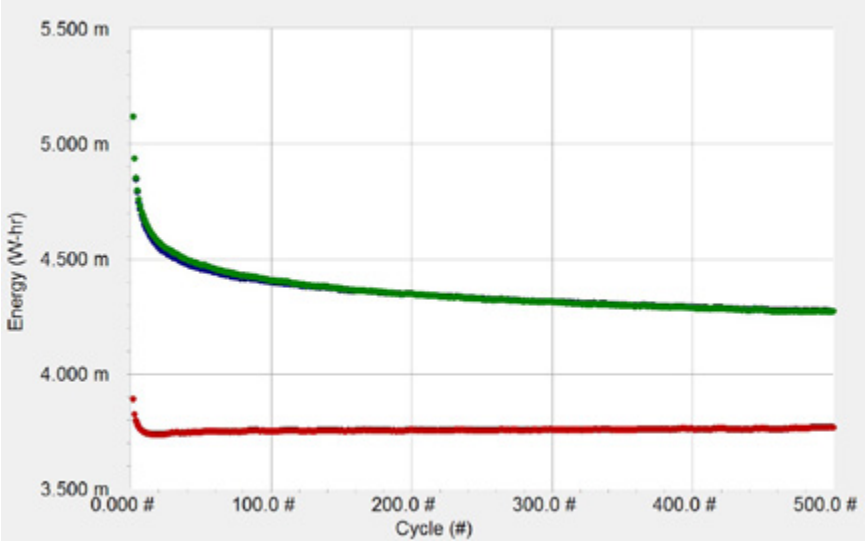
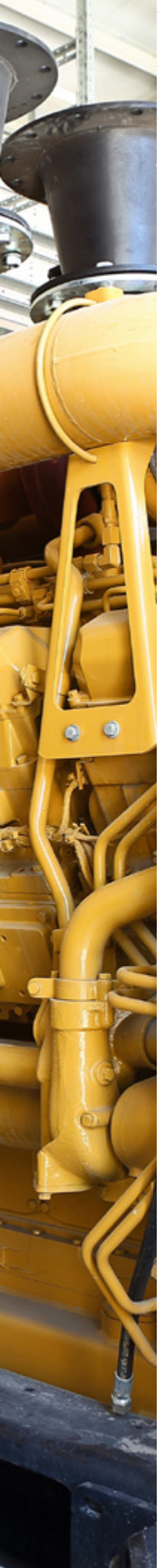


Figure 29. Charge energy versus cycle number of single cells in an unbalanced stack with two 3 F EDLCs (● C_1, ● C_2) and one 5 F EDLC (● C_3).

In a capacitor stack with unbalanced capacitor values, the capacitors with the highest capacitances have a lower effective voltage range. These deviations in voltage also lead to differences in energy.

The energy of the 5 F EDLC is reduced due to lower voltage limits. The two 3 F EDLCs try to balance this voltage loss with higher voltages. Their energy content increased.

In extreme cases, the voltage (and energy) increase can be large enough to damage the cells causing a safety hazard.



Unbalanced stack with different leakage resistances

Leakage resistance affects both stack performance and cycle-life. It can change as a capacitor ages. Low leakage resistances lead to higher leakage currents which discharge the cell without external current applied.

Leakage resistance can be modeled as a resistor parallel to a capacitor (see Figure 30).

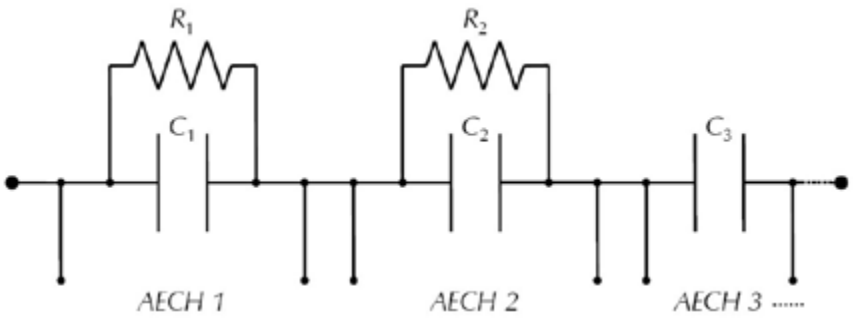


Figure 30. Diagram of serially-connected capacitors with Auxiliary Electrometer connections. Parallel resistors R_1 and R_2 simulate different leakage resistances.

Figure 31 shows the self-discharge from leakage current. Two resistors (R_1 = 16.5 kΩ, R_2 = 154 kΩ) were installed parallel to C_1 and C_2. The intrinsic leakage resistance for C_3 is in the MΩ-range. All three capacitors have a nominal capacitance of 3 F. The stack was charged to 8.1 V using a charge current of 0.225 A. After charging to 8.1 V the voltage was recorded in currentless state for 6 h.

Internal leakage current leads to a continuous voltage drift that discharges the cell. Capacitor C_1 with the lowest leakage resistance has the highest leakage current. It causes the highest loss in voltage (about 850 mV). In comparison, the total voltage-loss of the stack is about 1 V after 6 h.

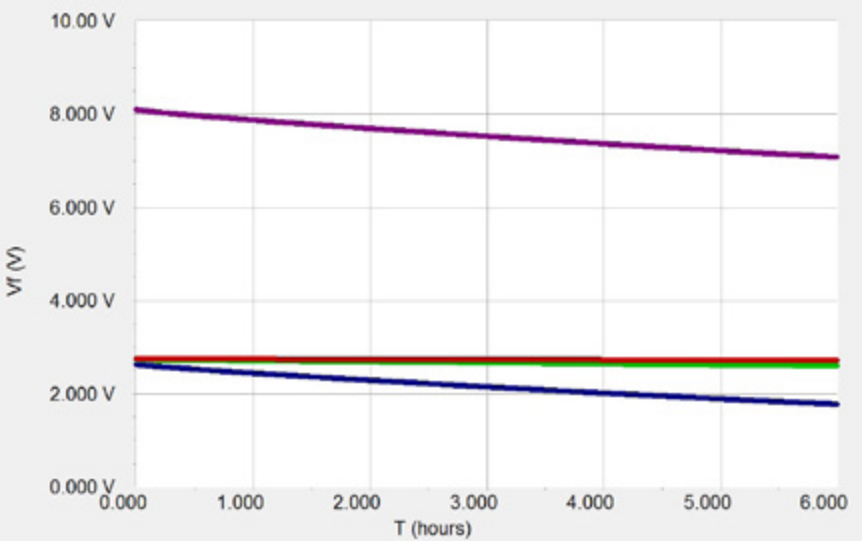
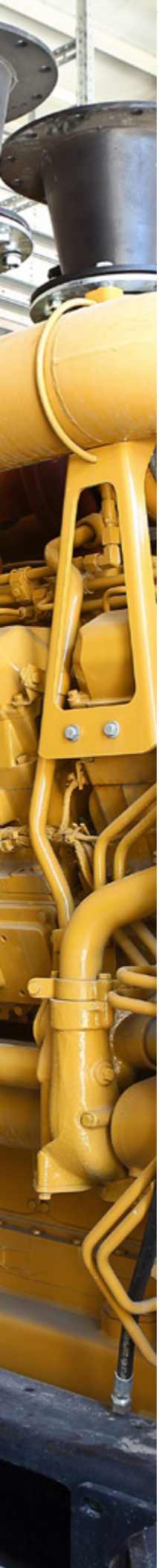


Figure 31. Self discharge over 6 hours of an unbalanced stack (●) and its single cells (● C_1, ● C_2, ● C_3) with different leakage resistances.



The calculated leakage current for C_1 is 47 μA whereas the other two capacitors exhibit values of only 7 μA (C_2) and 2 μA (C_3).

This measurement was done with a special self-discharge script in the software (Revision 5.61 and newer) named **PWR Self-Discharge.exp**

Higher leakage currents also lead to increased loss in energy and power. Figure 32 shows the behavior of energy during cycling. The prior stack setup was cycled for 500 cycles between 4 V and 8.1 V with a current of ±0.225 A.

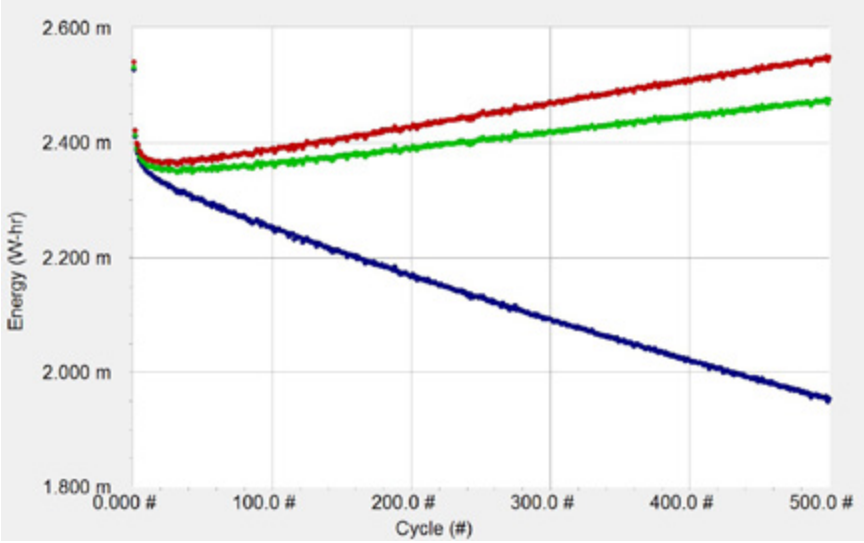


Figure 32. Charge energy versus cycle number of single cells (● C_1, ● C_2, ● C_3) with different leakage resistances in an unbalanced stack.

Higher leakage currents cause continuous energy-fade during cycling. The energy of C_1 decreases continuously caused by higher self-discharge. This is in contrast to Figure 25 and Figure 26, where voltage- and energy-imbalances were independent of the cycle number.

Capacitors C_2 and C_3 compensate for this loss and overcharge to higher voltages. Energy increases but this may be at the cost of lower electrochemical stability and decreased cycle-life.

Conclusion

This application note describes Gamry's CCD software by tests on single 3 F EDLCs and small stacks. Effects of different setup parameters on performance of EDLCs were presented and the influence of common irregularities in stacks was described. The combination of single-cell investigation and recording of multiple parameters enables accurate evaluation of irregularities in stacks.

Part 3: Electrochemical Impedance Spectroscopy

Introduction

Part 1 of this series of notes discusses basic theory of capacitors and describes several techniques to investigate electrochemical capacitors. Part 2 explains Gamry's Electrochemical Energy software for cycling of energy-storage devices. Effects of different parameters during cycling of single cells and stacks are described. Part three discusses the basics of Electrochemical Impedance Spectroscopy (EIS) and introduces Gamry's EIS techniques by measurements on single electrochemical capacitors (ECs) and stacks.

All parts of this white paper can be found in the Application Notes section of Gamry's website, www.gamry.com.

Experimental

Measurements were done on 3 F electric double-layer capacitors (EDLCs) (part #ESHSR 0003C0 002R7) and 5 F EDLCs (part #ESHSR 0005C0 002R7) from Nesscap[6], a 650 F EDLC (part #BCAP0650 P270) from Maxwell[7], and a 1 F PAS pseudocapacitor (part #PAS0815LR2R3105) from Taiyo Yuden[8]. The acronym PAS stands for Polyacenic Semiconductor, which is a conductive polymer deposited on the electrodes.

The data in this note were recorded using Gamry's Electrochemical Impedance 300 software and a Reference 3000. All plots were generated and evaluated using Gamry's Echem Analyst.

Electrochemical Impedance Spectroscopy

EIS is widely used to investigate electrochemical systems. The advantage of EIS is that it is generally non-destructive to the investigated system. This enables the possibility for further electrochemical measurements and post- mortem investigations.

6. Nesscap Energy Inc., 24040 Camino Del Avion #A118, Monarch Beach, CA, 92629.
7. Maxwell Technologies, Inc., 3888 Calle Fortunada, San Diego, CA, 92123.
8. Taiyo Yuden (U.S.A.) Inc., 497 Hooksett Road, PMB #38, Manchester, NH 03104.

EIS is the most common method for measuring the equivalent series resistance (ESR) of ECs. It also allows creating models to describe underlying reaction mechanisms. With these models capacitor non idealities can be investigated.

Generally, a sinusoidal AC excitation signal is applied to the investigated system during an EIS experiment, and the AC response is measured. The frequency of the input signal varies during the measurement. Finally, the impedance Z of the system is calculated, expressed in terms of magnitude Z_0 in Ω and phase-shift ø in degrees.

For basic information on EIS, see Gamry's application note at **www.gamry.com**, "Basics of Electrochemical Impedance Spectroscopy".

EIS Measurement Modes

Gamry's Electrochemical Impedance Spectroscopy Software can measure impedance spectra using four different modes:

- Potentiostatic
- Galvanostatic
- Hybrid
- OptiEIS

In potentiostatic mode, a DC voltage is applied that is superimposed by an AC voltage signal. The frequency of the signal is changed during the experiment and the phase-sensitive AC current response is measured.

Galvanostatic mode is similar to potentiostatic mode. In contrast, a DC current superimposed by an AC current signal is applied to the system, and the phase-sensitive AC voltage response is measured.

Hybrid EIS also uses galvanostatic cell control. In addition, the amplitude of the AC current is adjusted to maintain a nearly constant AC potential response.

Potentiostatic mode is most common in research. However, small errors in the applied DC voltage can lead to huge DC currents in low impedance cells, thus destroying the cell. Therefore galvanostatic and Hybrid EIS are preferred for low-impedance cells.

Three application notes give suggestions for making low impedance EIS measurements. You can find them at Gamry's website **www.gamry.com**:

"Accuracy of Contour Plots"

"Verification of Low Impedance EIS Using a 1 mΩ Resistor"

"Low-impedance EIS at its Limits with the Reference 30k Booster"

OptiEIS is a multisine technique and differs from the other methods described above. Instead of a single sinusoidal waveform with only one frequency, multiple waveforms with several frequencies are applied to the system simultaneously. Hence the time for EIS measurements can be reduced by up to a factor of four. OptiEIS can be run potentiostatically or galvanostatically.

For more information on multisine EIS, see Gamry's application note at ***www.gamry.com***: "OptiEIS: A Multisine Implementation"

Randles Model for Electrochemical Capacitors

The ideal capacitor does not exist: in reality, several effects lead to imperfections in the system. Hence, different models are used to describe the investigated system. The most common and simplest model fitted to EIS spectra of electrochemical capacitors is a simplified Randles model, shown in Figure 33:

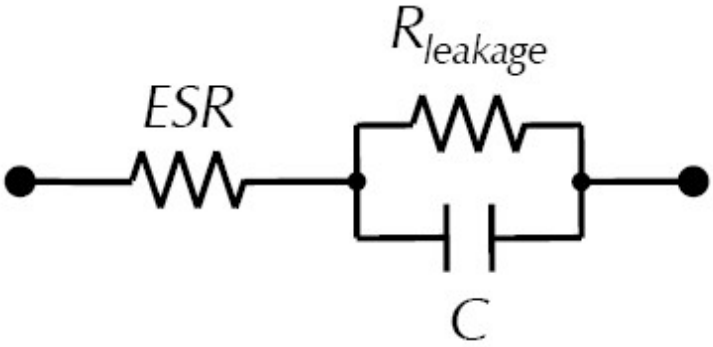


Figure 33. Diagram of a simplified Randles model.

The circuit elements in the model are:

- ESR Equivalent series resistance
- $R_{leakage}$ Leakage resistance
- C Ideal capacitance

The ESR is modeled in series to the ideal capacitance. Resistances from the electrolyte, the electrodes, and electrical contacts are summed in the ESR. A small ESR leads to better performances of energy-storage devices.

In contrast, a small leakage resistance $R_{leakage}$ leads to a higher leakage current, which is responsible for self-discharge of a charged capacitor when no external load is connected. The leakage resistance is modeled parallel to C.

Figure 34 shows a Bode plot of a Randles model in the frequency range between 10 kHz and 1 μHz. The fit parameters are typical values for electrochemical capacitors:

ESR 100 mΩ

$R_{leakage}$ 100 kΩ

C 1 F

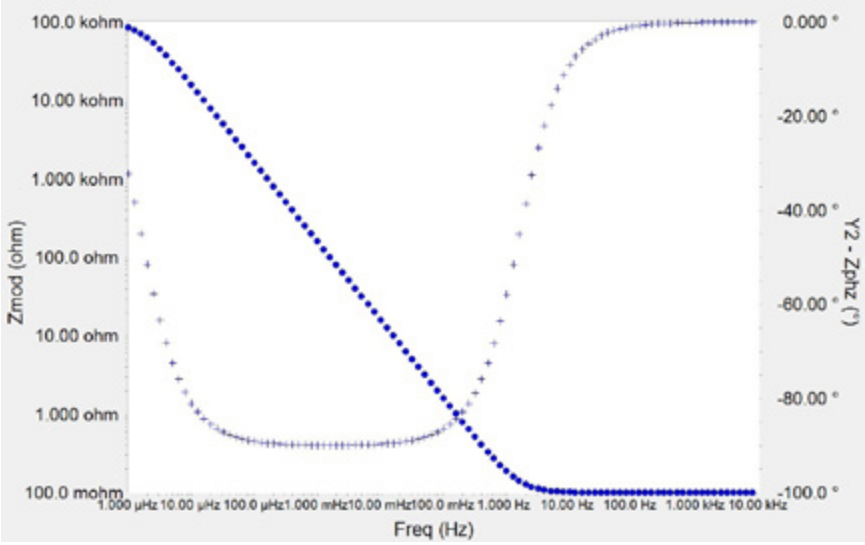


Figure 34. Bode plot of Randles model. (●) magnitude, (+) phase.

The Bode spectrum of a typical Randles model has three regions:

- Above 10 Hz, magnitude and phase approach 100 mΩ and 0° respectively. The ESR dominates this region.
- Between 100 μHz and 100 mHz, capacitance controls the impedance. Magnitude versus frequency is linear (on the log-log Bode plot) with a slope of –1 and the phase approaches –90˚.
- Below 10 μHz, the impedance begins a transition back towards resistive behavior as leakage resistance becomes dominant. This transition is incomplete even at 1 μHz.

EIS spectra of real devices rarely give much information about leakage resistance because its effects are seen at impractically low frequencies. Measurements at these frequencies take a long time.

Part 1 of this white paper describes in detail methods to measure leakage current.

Transmission-line Models for Electrochemical Capacitors

Real electrochemical capacitors do not show the simple behavior of a Randles model. Figure 35 shows a Bode plot of a 3 F EDLC. In addition, two different models are shown: the simplified Randles model (red curve) and the Bisquert Open model (green curve).

The impedance of the 3 F EDLCs used to generate data for this note is high enough that any control mode can be used. Because potentiostatic EIS is most common, this mode was used.

The capacitor was first charged to 2.7 V and held at this potential for 10 min. For the EIS experiment, DC voltage was set to 2.7 V superimposed by an AC voltage of 1 mV. The frequency ranged from 10 kHz to 100 μHz.

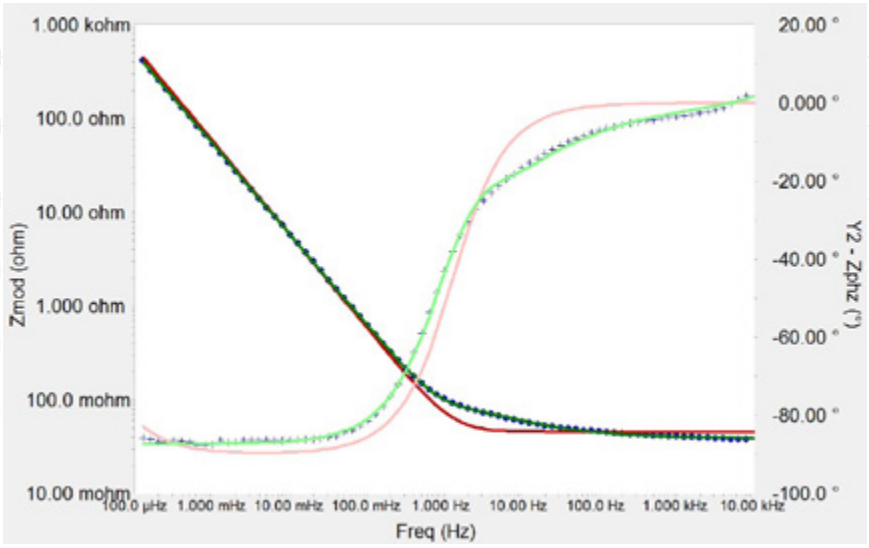


Figure 35. Bode diagram of a potentiostatic EIS test on a 3 F EDLC (●). (●) Randles model, (●) Bisquert open model. (●) magnitude, (+) phase.

As expected, fitting a Randles model to the spectrum shows poor agreement. The fit-results are

ESR	45.5 mΩ ± 0.2 mΩ
$R_{leakage}$	3.6 kΩ ± 0.4 kΩ
C	2.75 F ± 0.01 F

This result is typical for EIS spectra of electrochemical capacitors in which electrode porosity leads to very non uniform access of the electrolyte to the electrode surface, and Faradaic reactions occur. Simple resistor and capacitor models do not apply.

Differences between Randles model and real ECs include:

- Between 10 Hz and 10 kHz, magnitude is not constant but slightly increasing. The transition from resistive to capacitive behavior occurs in stages.
- Phase never approaches the simple model's 0˚ prediction at higher frequencies.
- No sign of leakage resistance is seen in this frequency range.

The fit to the data is much better using a porous-electrode transmission-line model. Figure 36 shows the Bisquert Open model that describes also electrode porosity.

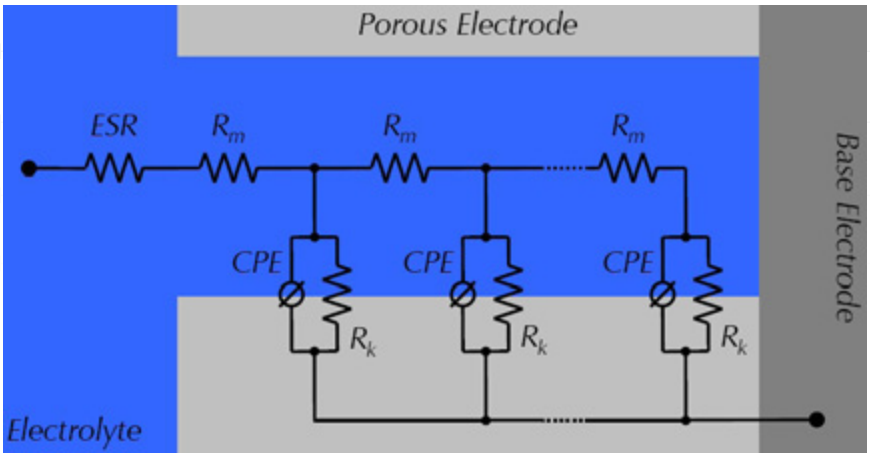


Figure 36. Diagram of the Bisquert open model.

Among ESR, a pore resistance R_m is added that increases with increasing pore depth. A Constant-Phase Element (CPE) replaces the ideal capacitance and defines inhomogeneities of the electrode surface in ECs. An interfacial resistance R_k similar to the leakage resistance is parallel to CPE and completes the model.

For more information on transmission-line models, see Gamry's application note at ***www.gamry.com***, "Demystifying Transmission Lines: What Are They, Why Are They Useful?"

The fit of the Bisquert open model in Figure 35 is represented in green. The fit-parameters are

ESR	38.2 mΩ ± 0.4 mΩ
R_m	96 mΩ ± 17 mΩ
R_k	1.3×10^{34} Ω ± 1×10^{38} Ω
Y_m (CPE)	2.54 S·s$^{\alpha}$ ± 0.15 S·s$^{\alpha}$
α(CPE)	0.97 ± 0.03

The Bisquert Open model complies much better with the Bode plot in Figure 32 than the Randles model, and it overlaps nearly perfectly.

Transmission-line models take into account the stepwise increase of the magnitude at higher frequencies. The transition region from resistive to capacitive behavior at frequencies above 100 mHz is described much better. Hence the fit-value for the ESR is smaller than the result of the Randles model.

The high uncertainty in the interfacial resistance R_k is expected. This resistance dominates the impedance in the low-frequency region that is not included in the spectrum.

EIS on a 3 F EDLC at Different Potentials

For ideal EDLCs, EIS spectra are independent of the applied DC voltage. However, real devices do not show this tendency.

Figure 37 shows Bode plots of a 3 F EDLC recorded at five different DC potentials: 0 V, 1 V, 2 V, 3 V, and 3.5 V. The last value is much higher than the 2.7 V specification of the EDLC.

The spectra were measured potentiostatically with an AC voltage of 1 mV_{rms} in a frequency range from 10 kHz to 10 mHz. The capacitor was held at the DC voltage for 10 minutes before each measurement.

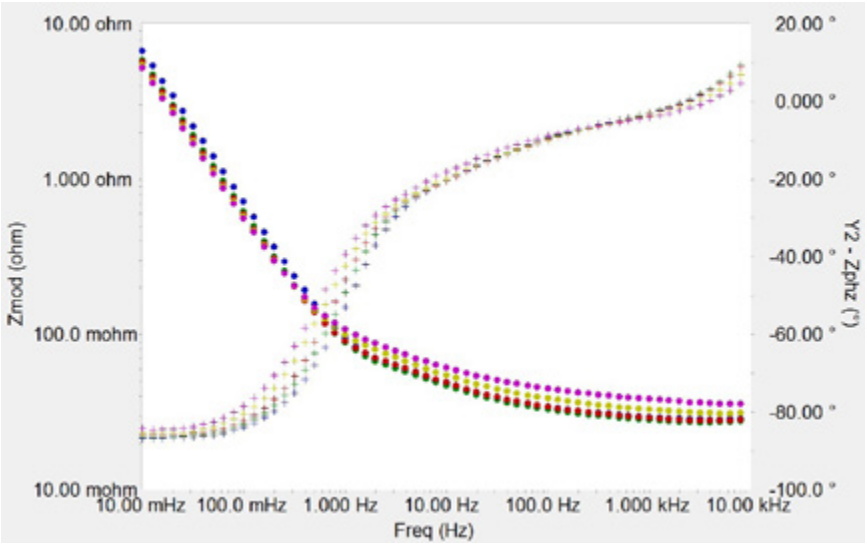


Figure 37. Bode diagrams of potentiostatic EIS tests on a 3 F EDLC. (●) 0 V, (●) 1 V, (●) 2 V, (●) 3 V, (●) 3.5 V. (●) magnitude, (+) phase.

Obviously, this EDLC shows non-ideality between 1 Hz and 10 kHz. Exceeding the rated voltage of the capacitor can cause decomposition and deposition reactions on the electrode surface. These irreversible Faradaic reactions can lead to an increase in ESR shown in the frequency range above 1 Hz where ESR dominates the impedance.

Below 1 Hz, impedance is decreasing with increasing voltage. In this frequency region, impedance depends on the DC voltage, so the capacitance increases and must also depend on DC voltage. Increased capacitances at higher potentials can be at the cost of shorter lifetimes.

EIS on a 1 F pseudocapacitor at different potentials

Just as for ideal EDLCs, EIS spectra recorded on an ideal pseudocapacitor should superimpose at different DC voltages. Yet for real pseudocapacitors this behavior does not apply.

Figure 38 shows Bode plots of a 1 F PAS pseudocapacitor recorded by potentiostatic EIS mode. The DC voltages were 0 V, 1 V, 2 V, and 2.4 V. The AC voltage was set to 1 mVrms. The frequency range was between 10 kHz and 10 mHz.

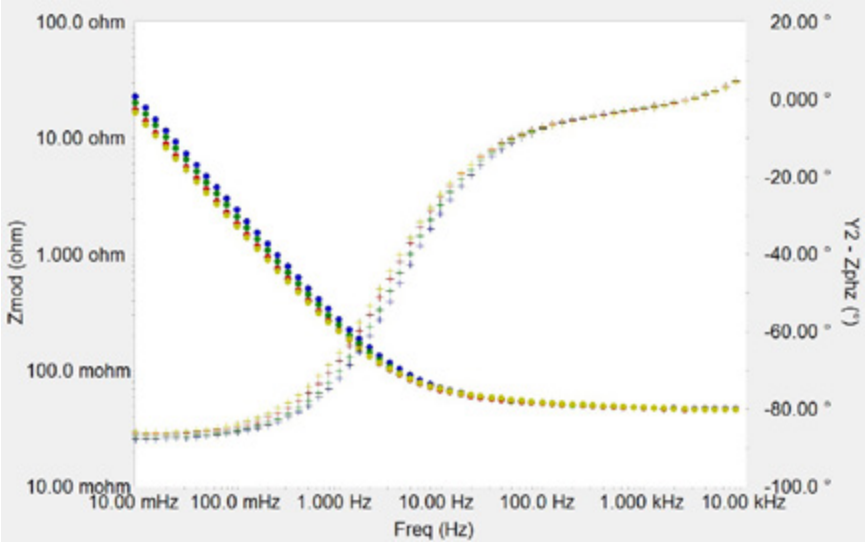


Figure 38. Bode diagrams of potentiostatic EIS tests on a 1 F PAS pseudocapacitor. (●) 0 V, (●) 1 V, (●) 2 V, (●) 2.4 V. (●) magnitude, (+) phase.

Just as for EDLCs, pseudocapacitors show voltage-dependence in impedance at lower frequencies. With increasing voltage, impedance decreases.

In contrast to the 3 F EDLC (Figure 37), this 1 F pseudocapacitor showed no voltage-dependence at frequencies above 10 Hz.

EIS on a Low ESR 650 F EDLC

EIS measurements on low-ESR capacitors are difficult. The technique generally requires:

- True 4-terminal measurements
- Galvanostatic cell control
- Low-resistance contacts
- Twisted-pair or coaxial cell leads

Figure 36 shows the connections used to record the EIS spectrum of a 650 F EDLC. 1.5 mm thick copper sheets were used for the connections. The current-carrying leads (green and red) and the voltage sensing leads (white and blue) are on opposite sides of the device.

Warning: Avoid shorting capacitor terminals though low-resistance connections. Very dangerous currents of hundreds or even thousands of ampères could flow.

Figure 39. Electrode connections for measurements on a 650 F EDLC. Working (green), Counter (red), Working sense (blue), and Reference (white).

Figure 40 shows a Hybrid EIS spectrum of a 650 F EDLC. The capacitor was first charged to 2 V and held at this potential for 30 min to maintain a constant voltage during the EIS measurement. The DC current was zero and the AC voltage was 0.1 mV_{rms}. The EIS spectrum was recorded from 1 kHz to 10 mHz.

Note that Hybrid EIS is still working in galvanostatic mode although an AC voltage is defined in the setup. The galvanostat modifies the AC current to maintain nearly the adjusted AC voltage response.

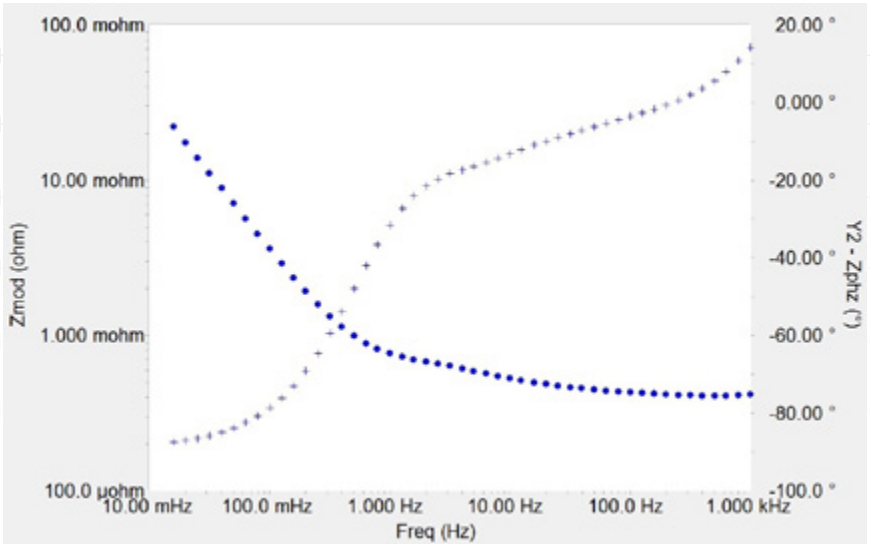


Figure 40. Bode diagram of a Hybrid EIS test on a 650 F EDLC. (●) magnitude, (+) phase.

This 650 F EDLC has a rated ESR of less than 600 $\mu\Omega$ at 1 kHz. The measurement yields a value of 418 $\mu\Omega$, which is less than this capacitor's rated ESR of 600 $\mu\Omega$.

Looking at the DC potential of the EDLC during the EIS measurement, it changes only by about 2 mV, which is necessary for reliable results.

OptiEIS: a Multisine Technique

Gamry's OptiEIS enables the user the possibility to perform EIS measurements faster than with conventional single-sine techniques.

Figure 41 shows Bode plots of a potentiostatic EIS test and an OptiEIS experiment in potentiostatic mode on a 3 F EDLC. The capacitor was first charged to 2.7 V and held at this potential for 20 minutes. A DC voltage of 2.7 V and an AC voltage of 10 mV were applied. The frequency ranged from 40 Hz to 10 mHz.

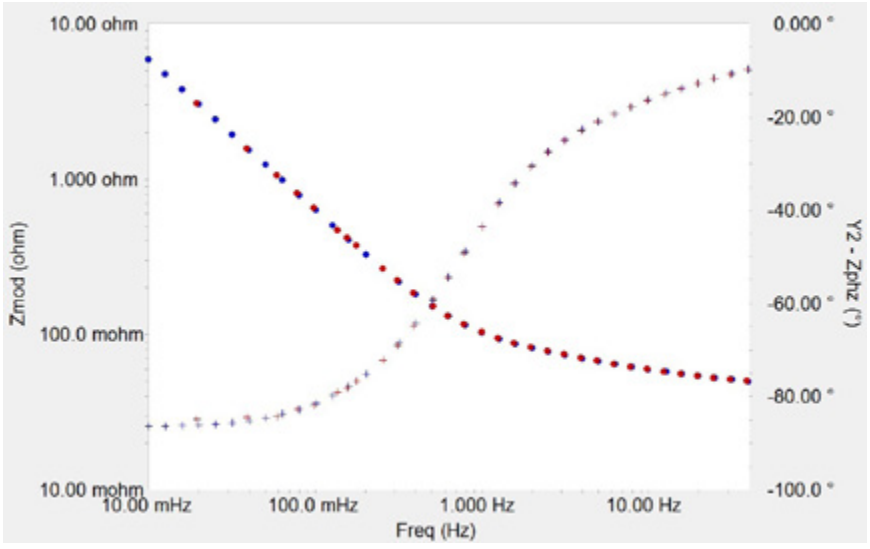


Figure 41. Bode diagrams of a potentiostatic EIS test (●) and an OptiEIS test (●) on a 3 F EDLC. (●) magnitude, (+) phase.

Both Bode plots of the potentiostatic EIS and OptiEIS experiments overlap perfectly. In low-noise mode, the potentiostatic EIS test takes about 30 min. With OptiEIS, measurement time is reduced to only 9 min, which is a factor of about three in reduction.

EIS during Cycling Experiments

EIS can be combined with other techniques, such as cyclic charge-discharge (CCD) tests. This combination enables investigation of changes in a system with time. For detailed information about practical applications and evaluation of CCD tests see Part 2 of this white paper.

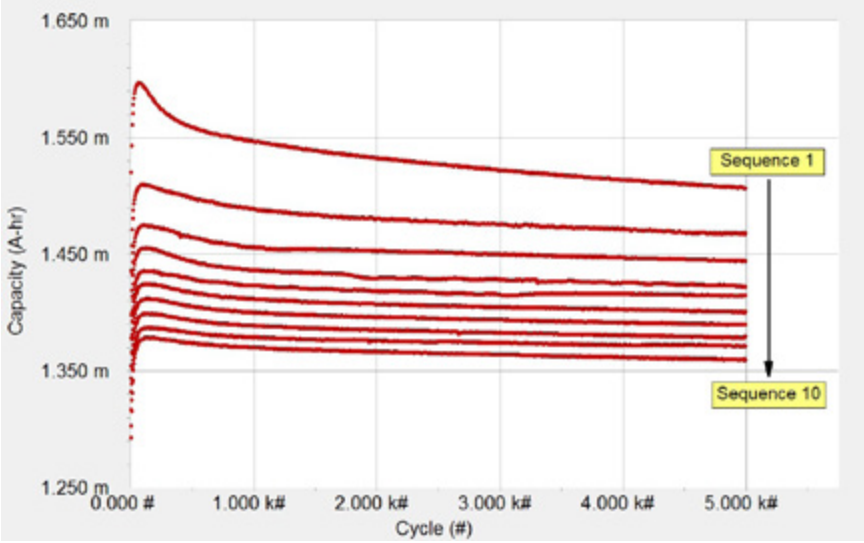


Figure 42. CCD test on a 3 F EDLC over 50 000 cycles interrupted by galvanostatic EIS experiments. For details, see text.

Figure 42 shows the changes of capacity during a CCD experiment. Ten sequences were run; each had 5000 cycles. Prior to the first cycle, and after each sequence, a galvanostatic EIS experiment was performed. The total number of cycles was 50,000.

To perform complex sequences, Gamry offers the Sequence Wizard. It allows building of individual sequences with a wide spectrum of techniques. For more information about the Sequence Wizard, visit Gamry's website ***www.gamry.com***.

For the CCD test, a 3 F EDLC was first charged to 1.35 V and then cycled between 1.35 V and 3.5 V with a current of ±2.25 A.

Capacity decreases with increasing cycle number. Because the upper voltage limit of 3.5 V is way above the limitations of the EDLC, irreversible reactions on the electrode surface can occur, which decrease the performance.

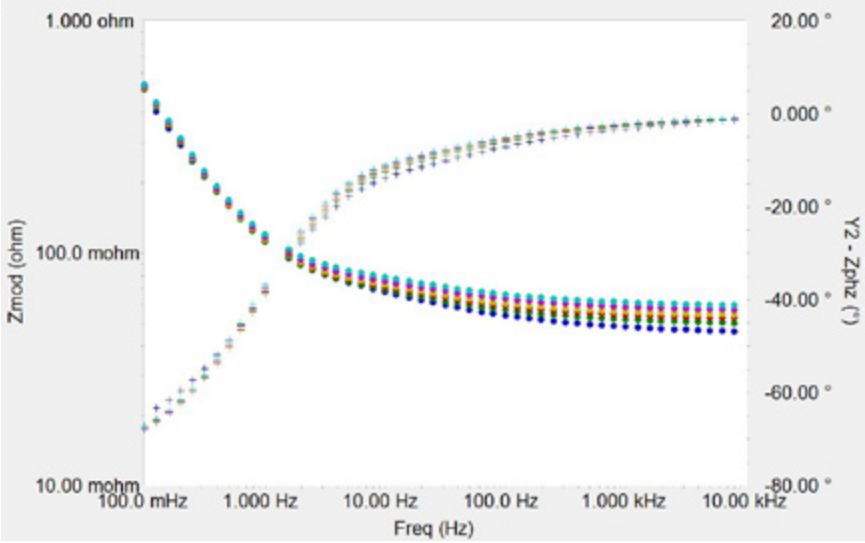


Figure 43. Bode diagrams of galvanostatic EIS tests on a 3 F EDLC during cycling. (●) 1st cycle, (●) 10 000th cycle, (●) 20 000th cycle, (●) 30 000th cycle, (●) 40 000th cycle, (●) 50 000th cycle. (●) magnitude, (+) phase.

Figure 43 shows the Bode plots. Zero DC current and 10 mA_{rms} AC current were applied. The spectra were recorded from 10 kHz to 100 mHz. Prior to each EIS test, the potential was held at 3.5 V for four hours.

Note: The hold step is necessary, keeping the system in a steady state during the galvanostatic EIS measurement, to fulfill the stability criterion for EIS.

Impedance increases in the frequency range between 1 Hz and 10 kHz with increasing cycle number. In this region ESR dominates the impedance. Evaluation of the fits for these spectra confirms that the ESR increases. After 50 000 cycles the ESR increased by about 14 mΩ, an increase of more than 30%.

In contrast, capacitance decreases with increasing cycle number caused by irreversible reactions that can occur on the electrode surface.

Table 2 lists the fit values for the ESR and capacitance, dependent on the cycle number.

Cycle #	1	10k	20k	30k	40k	50k
ESR (mΩ)	44.5	48.7	51.4	53.1	55.8	58.4
C (F)	3.01	2.94	2.90	2.87	2.84	2.81

Table 2. Change in ESR and capacitance versus cycle number.

EIS on Stacks

Single energy-storage devices are stacked together for high voltage applications. For this, cells are connected in serial and parallel circuits. For further information about cell stacks see Part 2 of this white paper.

Figure 44 shows a test setup for stack measurements used in this note. It consists of a serial connection of two 3 F EDLCs and one 5 F EDLC. A higher ESR is simulated for the second capacitor with a 0.5 Ω resistor in series. The voltage of each single cell was measured with individual channels of Gamry's Auxiliary Electrometer.

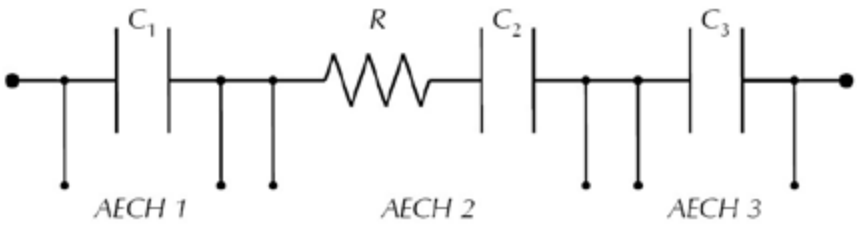


Figure 44. Serially connected capacitors with Auxiliary Electrometer connections (AECH 1, AECH 2, and AECH 3). Serial resistor R simulates a higher ESR.

For the EIS experiments with a stack, every single cell was initially charged to 1 V. After this, the stack was charged to 9 V with a current of 3 A. The potential was held for 20 minutes prior to the EIS measurement.

Figure 43 shows Bode plots of the stack and all three single cells that were recorded simultaneously with the Auxiliary Electrometer. The EIS experiment was performed in galvanostatic mode with zero DC current and 10 mA_{rms} AC current. The frequency ranged from 10 kHz to 1 mHz.

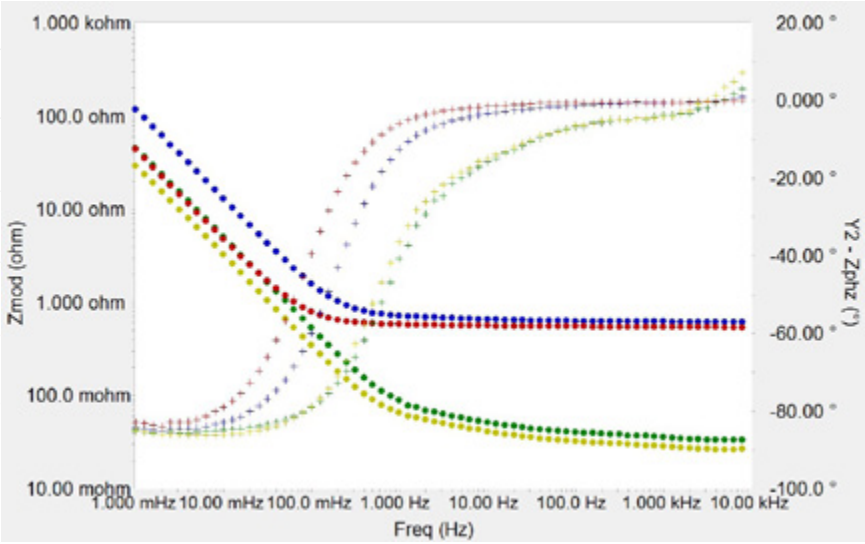


Figure 43. Bode diagrams of a galvanostatic EIS test on a stack of EDLCs. (●) stack, (●) C_1, (●) C_2 + R, (●) C_3. (●) magnitude, (+) phase.

At frequencies above 1 Hz, differences in ESR of each single cell can be seen. As the total voltage U of the stack, also the total ESR is the sum of the parameters of each single cell. Hence spectra are shifted upwards above 1 Hz with increasing ESR.

In contrast, the total capacitance C of a stack is the inverse of the sum of the reciprocal single capacitances. Hence total C is lower than the single capacitances. Below 100 mHz, in the linear region of the magnitude, spectra are shifted towards the bottom-left corner of the diagram with increasing capacitance.

Table 3 summarizes some parameters of the investigated stack and its single cells. ESR and capacitance C were calculated by fits from each EIS spectrum. The potential V was recorded during the charge step.

Element	***V (V)***	***ESR (mΩ)***	***C (F)***
Stack	9.00	613	1.27
C_1	2.78	35.7	3.28
C_2 + R	3.55	543	3.49
C_3	2.67	31.2	5.01

Table 3. Measured parameters of the stack and its single cells.

Looking only at the parameters of the stack does not reveal imbalances of single cells. For example, if the stack were perfectly balanced and charged to 9 V, all single capacitors would be evenly charged to 3 V.

Because of unbalanced cell parameters (e.g., different ESR and different capacitances), the charge potentials of the single cells vary. You cannot see these differences in the total stack voltage, which is still 9 V.

Because capacitor C_2 has the highest simulated ESR, it overcharged by more than 0.5 V, whereas C_1 and C_3 did not reach the desired potential. Overcharging can damage a cell and drastically reduce performance and lifetime.

By using the Auxiliary Electrometer, the whole stack and each single cell can be investigated simultaneously. In this way, imbalances in capacitances, ESR, and cell potentials can be observed. The stack can be balanced by adjusting these parameters.

Conclusion

This white paper discusses theory and practice of EIS measurements with electrochemical capacitors. We showed that EIS is an indispensable tool to investigate energy-storage devices. Two models were explained to fit Bode spectra of ECs. For reliable fitting, transmission-line models are necessary to describe the porosity of high surface electrodes used in ECs.

Based on several measurements on ECs, different techniques were described: potentiostatic EIS, galvanostatic EIS, Hybrid EIS, and Gamry's multisine technique called OptiEIS. To show the wide variety of EIS applications, CCD tests were combined with EIS measurements to monitor changes in the system over time.

Finally, stack measurements were performed using Gamry's Auxiliary Electrometer. In this way, single cells of a stack can be investigated simultaneously in order to balance individual cell parameters.

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